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Comparative study on various PWM Strategies for Novel Multilevel Inverter

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Abstract : Multilevel Inverters offer high power capability, associated with lower output harmonics. This paper presents the performance analysis of new symmetrical multilevel inverter using different PWM strategies based on control freedom degree approach. These PWM strategies include carrier overlapping, variable frequency, phase disposition and phase opposition disposition pulse width modulation. The total harmonic distortion, V_{RMS}, Crest factor and Form factor are evaluated for various modulation indices. Simulations were performed using MATLAB-SIMULINK. It is observed that PODPWM strategy provide output with relatively low distortion and COPWM is found to perform better since it provides higher fundamental RMS output voltage.

Keywords *- CFD, PWM, THD, FF, and* V_{RMS}

I. INTRODUCTION

The recent development of new power semiconductor technologies offer capable of handling higher voltage and current rating enabled power electronic devices to be employed in applications with ever increasing power levels. But it is hard to connect single power semiconductor device directly to higher voltage level due to this multilevel inverter has emerged solution for working in the higher voltage levels. A Multilevel Inverter is a power electronic system that synthesis a desired output voltage wave from several outputs. By this several levels, we can achieve good power quality, output with low harmonic distortion, better electromagnetic capability and lower switching losses. Multilevel Inverter is extensively used in medium voltage levels with high power applications. The different topologies have been proposed for multilevel inverters diode clamped, capacitor clamped and cascaded inverter topology. Conventional H Bridge inverters are used in industrial side because of simple switching configuration and easy way of controlled. However harmonic components and switching losses are quite high. To obtain a more accurate wave form with minimum losses, the number of levels should be increased with reduce the number of switches. In this paper a new symmetrical multilevel inverter with reduced number of switches for 7 level inverter has been investigated through different PWM techniques. Multilevel inverter can be operating at both fundamental switching frequency and high switching frequency PWM. The high switching frequency PWM is classified as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM. Berrezzek Farid & Berrezzek Farid [1] made study on the various techniques of controlled PWM. Carrara et al [2] analysed three PWM methods with different vertical and horizontal combinations leading to the quantification of their output harmonics. Deng et al [3] and B.P Mcgrath et al [4] investigated multilevel PWM methods based on control degrees of freedom combination and its analysis. Martina calasis et al [5] discussed the multicarrier PWM scheme for H bridge cascaded inverter. Panda and Tripathi [6] presented a symmetrical hybrid sine PWM switching technique for full bridge inverter. Hybrid PWM switching not only reduces switching loss but also reduces circuit complexity. Rodriguez et al [7] described the classification of high switching frequency PWM as multilevel carrier based PWM and selective harmonic elimination. Shanthi and Natarjan [8] made a comparative as various carrier overlapping pulse width modulation techniques. Urmila and subbarayaudu [9] also made a comparative study on various pulse width modulation techniques. Wu et al [10] proposed a novel clew for the research on carrier based PWM methods for multilevel inverters based on the concept of combination of the Control Freedom Degrees (CFD).

This paper analysis a comparative study carried out on various bipolar PWM strategies for new Symmetrical multilevel inverter. Simulation is performed using MATLAB-SIMULINK.

II. NEW SEVEN LEVEL MULTILEVEL INVERTER TOPOLOGY

This new multilevel inverter has 4 main switches Q1 to Q4 and four auxiliary switches Q5 to Q8, three equal number of DC source, and therefore it is called as Symmetrical multilevel inverter. This topology can be extended up to n number of levels. The multilevel inverter operating modes are according to the polarity of load voltage and current.

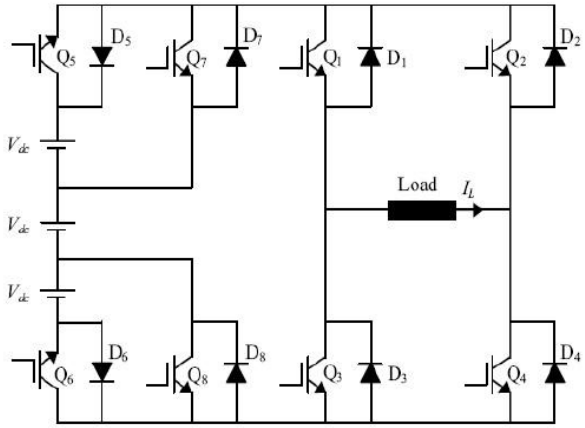


Fig. 1: New Seven level Symmetrical Multilevel Inverter
The seven voltage levels ($3V_{dc}$, $2\ V_{dc}$, V_{dc}, 0,- V_{dc},-$2\ V_{dc}$,-$3\ V_{dc}$) are generated as follows.

a. Output Voltage 3 V_{dc} : Auxiliary switches Q5,Q6 is ON, Load terminal positive is connected to main switch Q1and negative terminal to Q4.Now the circuit operation becomes Q5,Q1,load,Q4 and Q6.Now all the three sources are connected in series, therefore we obtained $3\ V_{dc}$.

b. Output Voltage 2 V_{dc}: Auxiliary switch Q5 is ON and the load is connected to Q1 with respect to Q4.Now the upper two sources are connected in series via Q5, Q1, Load, Q4, and D8.We get $2\ V_{dc}$ as an output voltage.

c. Output voltage V_{dc}: Diodes D7, D8 is ON the load is connected to Q1 with respect to Q4. The current path flow is D7, Q1, Load, Q4 and D8..Now the only one source is connected, and thus we obtain V_{dc}.

d. Output voltage Zero: Auxiliary switch Q7 or Q8 is alone in ON state.

In the negative half cycle (-V_{dc},-$2\ V_{dc}$ and -$3\ V_{dc}$) the main switches Q2 and Q3 is in ON state instead of Q1 and Q4 the remaining switches operation are similar to the first three stages mentioned above.

III. PULSE WIDTH MODULATION STRATEGIES

A number of modulation strategies are used in multilevel inverter. They can be classified as Fundamental Switching strategies, Space vector PWM strategies and Carrier based strategies. Out of three strategies, Fundamental switching strategies and space vector strategies are complicated when number of levels high.

The carrier based PWM is preferred for this proposed topology. Carrier based PWM strategies have more than one carrier that can be triangular waves or sawtooth waves and so on. As far as the particular carrier signals are concerned, there are multiple control degrees of freedom including frequency, amplitude, phase of each carrier and offsets between carriers. The reference wave of multilevel carrier based PWM strategies can be sinusoidal or trapezoidal. This paper focuses on the following four types of multicarrier PWM strategies.

- Phase Disposition PWM strategy (PDPWM)
- Phase Opposition and Disposition PWM strategy (PODPWM)
- Variable frequency PWM strategy (VFPWM)
- Carrier Overlapping PWM strategy (COPWM)

For an m level inverter, m-1 carriers with same frequency f_c and same peak to peak amplitude A_c are used. The reference waveform has amplitude Am and frequency fm and it is centred at zero level. The reference wave is continuously compared with each of the carrier signals. If reference wave is more than a carrier signal, than the active devices corresponding to that carrier are switched ON otherwise, the devices switch OFF.

The modulation index m_a is defined as

$m_a = 2\ A_m / (m-1)A_c$ except for COPWM strategy

The frequency ratio m_f is defined as $m_f = f_c/f_m$

3.1 Phase Disposition strategy:

In this method all the carriers above and below zero reference line are in same phase. If all the carriers are selected with the same frequency, amplitude and phase but they are different in DC offset. Carrier and reference wave arrangements are as shown in Fig.2.

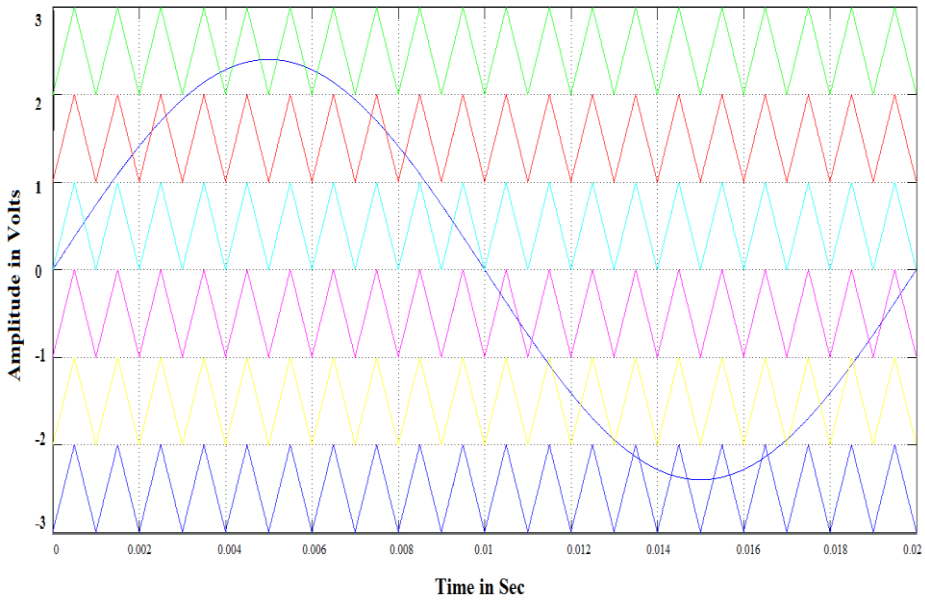


Fig. 2: Carrier arrangement for PDPWM strategy (m_a=0.8 and m_f=20)

3.2 Phase Opposition Disposition Strategy:

In this strategy, all the carriers have same frequency and amplitude, but all the carriers above the zero reference are same in phase and below the zero reference carriers also in phase but they are 180 degree phase shifted with respect to above reference.

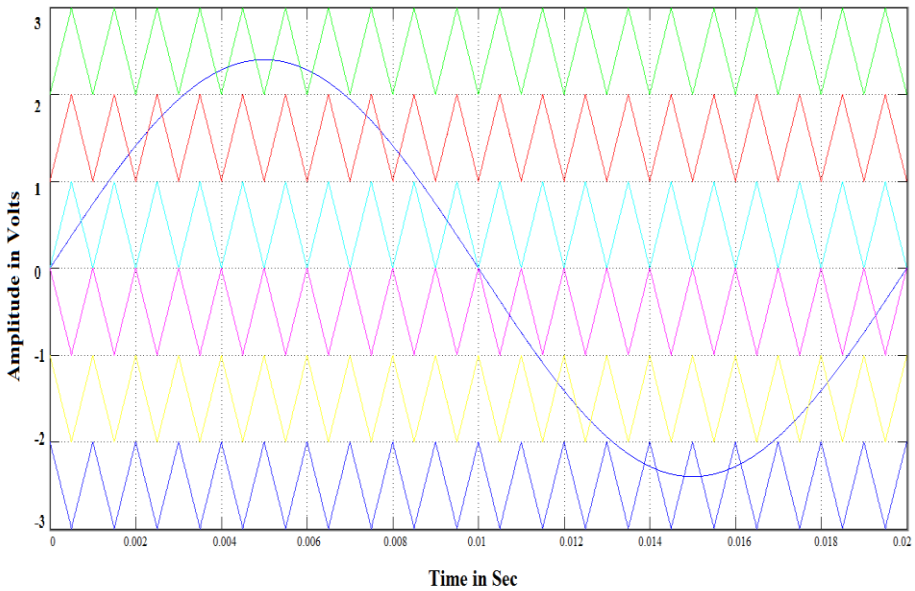


Fig. 3: Carrier arrangement for PODPWM strategy (m_a=0.8 and m_f=20)

3.3 Variable Frequency PWM (VFPWM) Strategy:

In this strategy all the carriers are in phase, same amplitude, with different frequency. The number of switching for upper and lower devices is chosen in multilevel inverter is much more than that of intermediate switches in PDPWM using constant frequency carriers. In order to equalize the switches variable frequency PWM strategy is preferred.

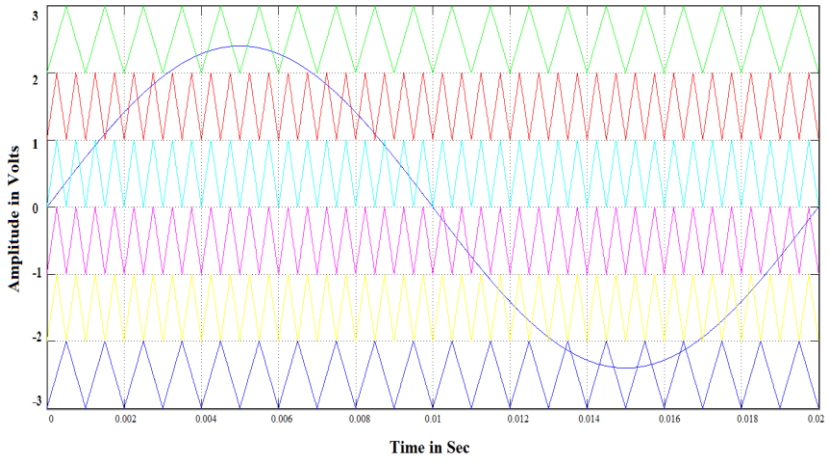


Fig. 4: Carrier arrangement for VFPWM strategy (m_a = 0.8, m_f = 20 and m_f = 40)

3.4 Carrier Overlapping PWM (COPWM) Strategy:

In carrier overlapping technique, carriers with the same frequency and same peak to peak amplitude are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform is centred in the middle of the carrier signals.

The modulation index m_a is defined as $m_a = 2\ A_m / (m - 3)A_c$

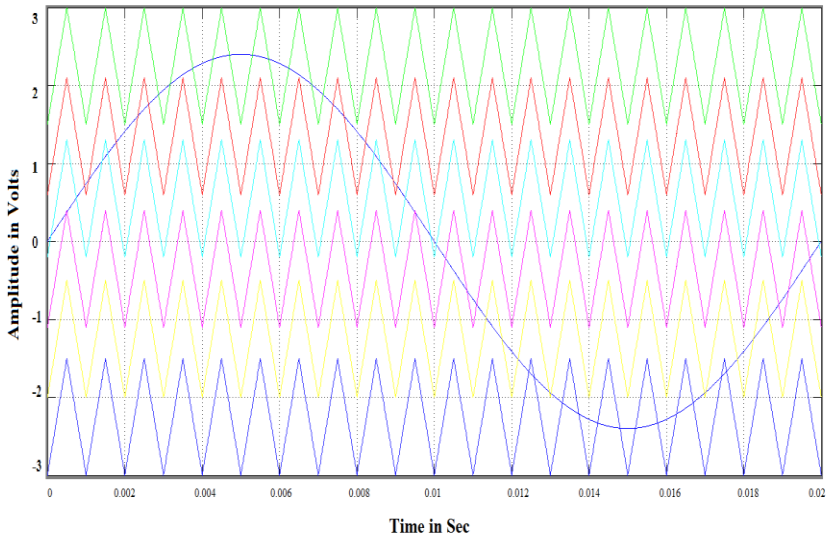


Fig. 5: Carrier arrangement for COPWM strategy (m_a=0.8 and m_f=20)

IV. SIMULATION RESULTS

The new symmetrical seven level multilevel inverter is modelled in SIMULINK using power system block set. Simulations are performed for different values of m_a ranging from 0.7 to 1 and the corresponding %THD is measured using the FFT block and their values are shown in "Table 1". "Table 2, 3 and 4 "shows the $V_{RMS,}$ Form Factor and Crest factor values.

"Figs 6-13" shows the simulated output voltage with above strategies but for only one sample value of $m_a = 0.8$. "Fig.6" shows the seven level output voltage generated by PDPWM strategy and its FFT plot is shown in "Fig 7". From "Fig.7", it is observed that the PDPWM strategy produces significant 6^{th} ,8^{th} , 14^{th} and 20^{th} harmonic energy. "Fig 8" shows the seven level output voltage generated by PODPWM strategy and its FFT plot is shown in "Fig. 9". From "Fig. 9" it is observed that the PODPWM strategy produces significant 9^{th} ,15^{th} and 19^{th} harmonic energy. "Fig 10" shows the seven level output voltage generated by VFPWM strategy and its FFT plot is shown in "Fig. 11". From "Fig. 11" it is observed that the VFPWM strategy produces significant 16^{th},18^{th} and 20^{th} harmonic energy.

"Fig 12" shows the seven level output voltage generated by COPWM strategy and its FFT plot is shown in "Fig. 13". From "Fig. 13" it is observed that the COPWM strategy produces significant 20^{th} harmonic energy. "Fig 14" Shows the comparison of % THD for modulation index values.

The following parameter values are used for simulation: V_{dc} = 100V, Resistive load – 10ohms, f_m = 50 Hz, fc = 1000Hz and 2000Hz.

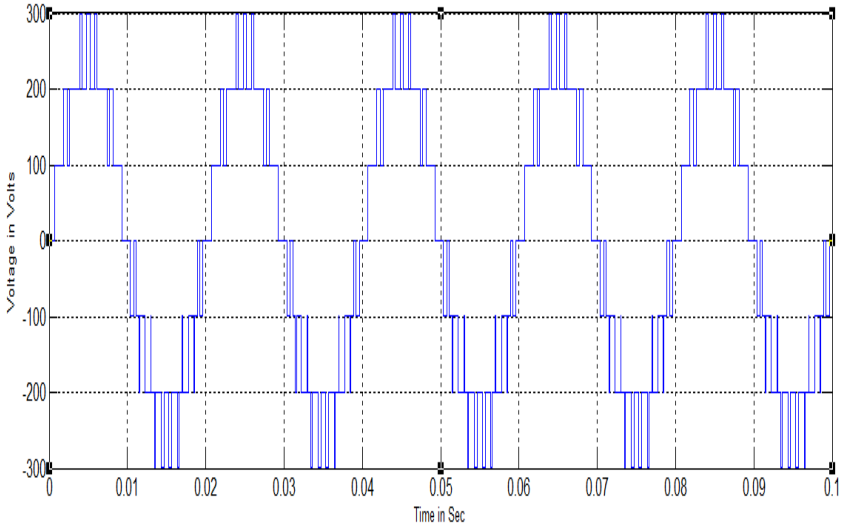


Fig. 6: Output voltage generated by PDPWM strategy

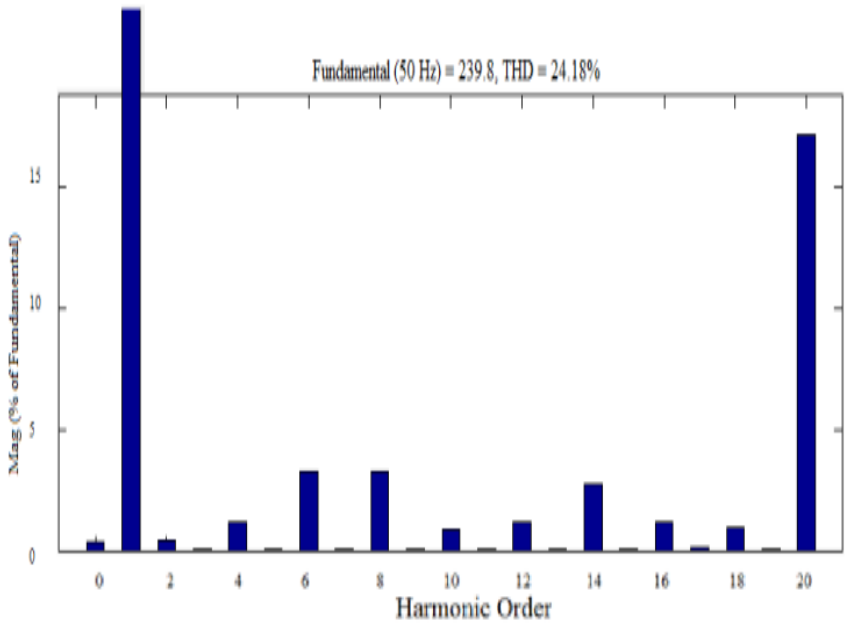


Fig. 7: FFT plot for output voltage of PDPWM strategy

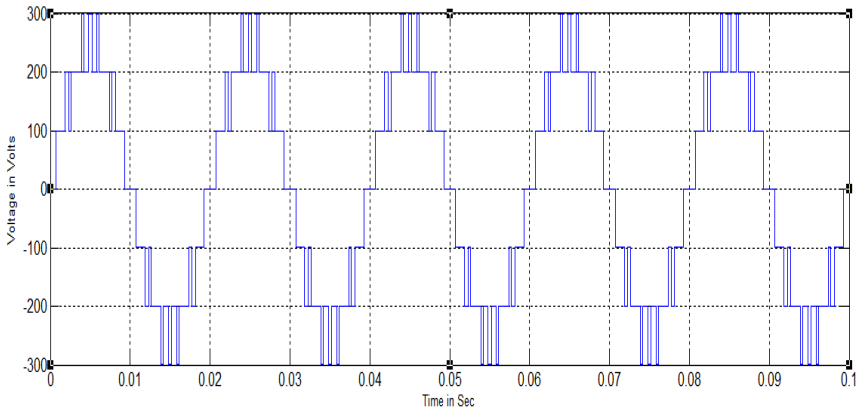


Fig. 8: Output voltage generated by PODPWM strategy

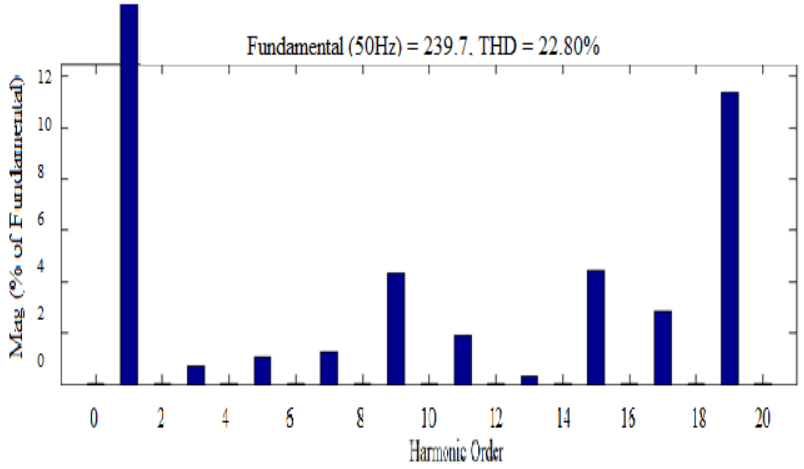
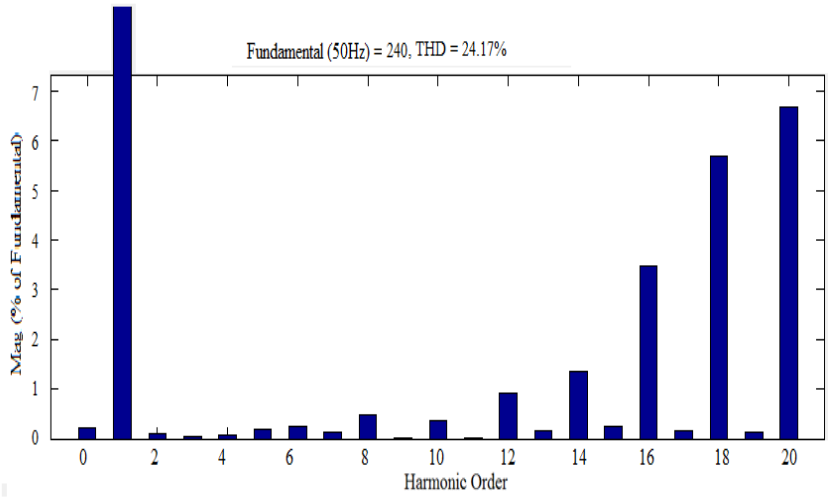


Fig. 9: FFT plot for output voltage of PODPWM strategy

Fig. 10: Output voltage generated by VFPWM strategy



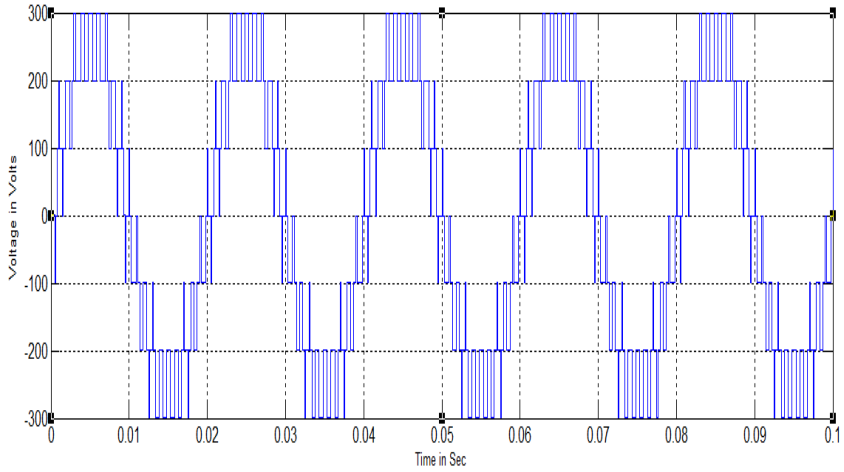


Fig. 11: FFT plot for output voltage of VFPWM strategy

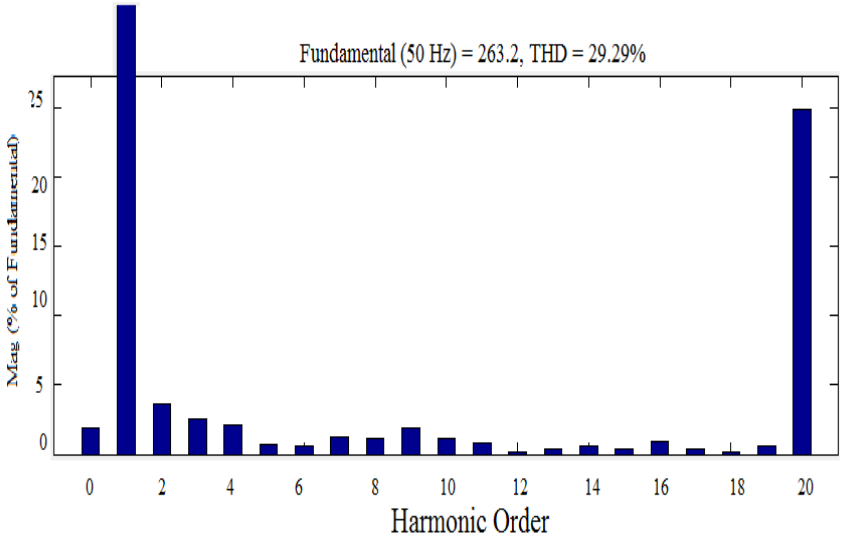


Fig. 12: Output voltage generated by COPWM strategy

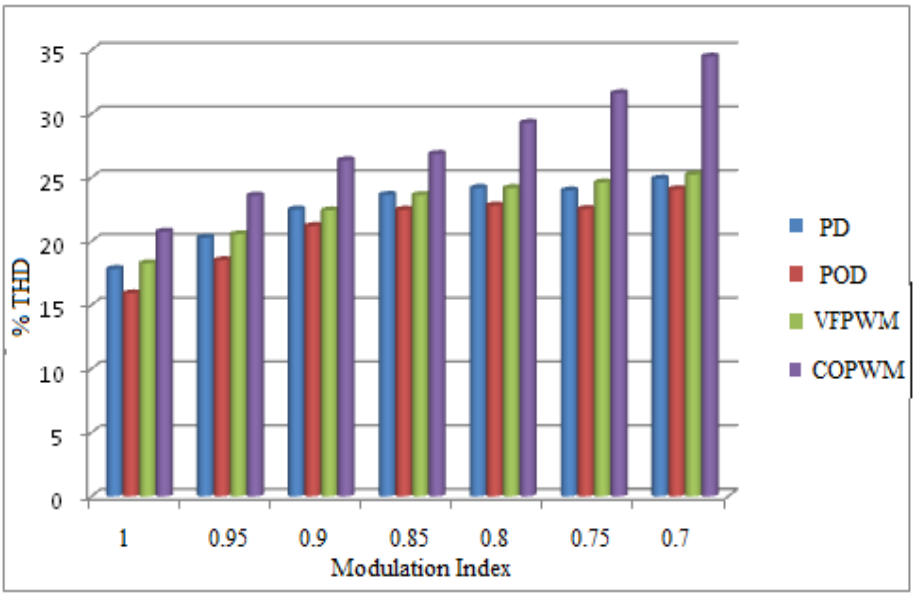


Fig. 14: %THD Vs ma for all strategies.

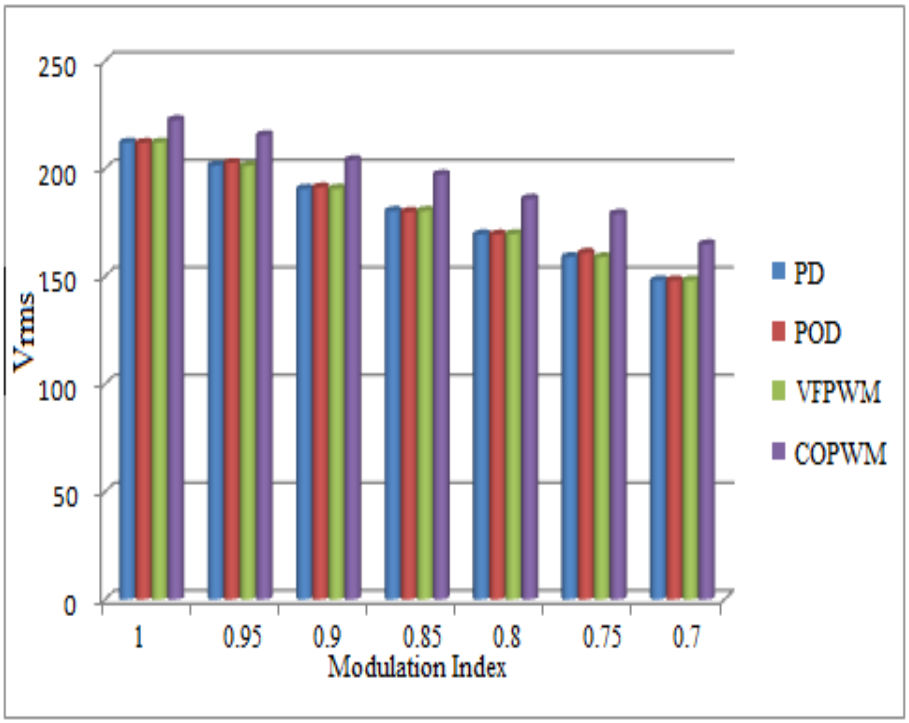


Fig. 15: V_{rms} Vs ma for all strategies.

TABLE 1: % THD for different modulation indices

Ma	PD	POD	VF	CO
1	17.82	15.91	18.27	20.75
0.95	20.28	18.51	20.55	23.58
0.9	22.49	21.20	22.42	26.36
0.85	23.63	22.47	23.62	26.84
0.8	24.18	22.8	24.17	29.29
0.75	23.98	22.53	24.61	31.61
0.7	24.91	24.08	25.23	34.48

TABLE 2: V_{RMS} (fundamental) for different modulation indices

Ma	PD	POD	VF	CO
1	212.2	212	212.2	222.6
0.95	201.5	202.7	201.4	215.6
0.9	190.7	191.4	190.8	204.1
0.85	180.4	180	180.5	197.3
0.8	169.6	169.5	169.7	186.1
0.75	159	161	158.9	179.1
0.7	148.2	148.2	148.2	165

TABLE 3: Form factor for different modulation indices

Ma	PD	POD	VF	CO
1	212	inf	2122	200.54
0.95	503.75	inf	1258.75	109.44
0.9	488.97	inf	1467.69	146.8
0.85	295.73	inf	1002.77	91.76
0.8	484.57	inf	737.82	97.94
0.75	283.92	inf	2270	56.67
0.7	871.76	inf	570	77.10

TABLE 4: Crest factor for different modulation indices

Ma	PD	POD	VF	CO
1	1.414	1.414	1.414	1.414
0.95	1.414	1.414	1.414	1.414
0.9	1.414	1.414	1.414	1.414
0.85	1.414	1.414	1.413	1.414
0.8	1.414	1.414	1.414	1.414
0.75	1.414	1.414	1.422	1.414
0.7	1.414	1.414	1.414	1.414

V. CONCLUSION

In this work the simulation results of single phase seven level new symmetrical multilevel inverter with resistive load with various modulating strategies are obtained through MATLAB/SIMULINK, various performance measures like THD, V_{RMS} , form factor and Crest factor were obtained and tabulated. It is observed from "Table.1" that PODPWM method provides output with relatively low distortion. The maximum DC utilization achieved in COPWM ("Table.2").

REFERENCES

[1] Berrezzek Farid and Berrezzek Farid, **"**A Study of New Techniques of Controlled PWM Inverters**",** *European Journal of Scientific Research, ISSN 1450-216X, Vol.32, No.1, pp.77-87., 2009*

[2] G.Carrara, S.Gardella, M.Marchesoni, R.Salutari and G.Seiutto: "A New Multilevel inverter PWM method: A theoretical analysis", *IEEE Transaction on Power Electronics vol 7, pp 497-505, July 1992.*

[3] Deng, Y. Wang, H. Zhang, C. Hu, L and He, X. "Multilevel PWM Methods based on Control Degrees of Freedom Combination and Its Theoretical Analysis",*IEEE Conf. Rec: 0-7803-9208-6/05, pp. 1692-1699, 2005.*

[4] B.P.McGrath and D.G.Holmes "Multicarrier PWM strategies for multilevel inverter" *IEEE Transactions on Industrial Electronics vol49, No.4, pp858-867, Aug 2002.*

[5] Martina Calais, Lawrence J. Borle and Vassilios G. Agelidis., "Analysis of multicarrier PWM methods for a single phase five level inverter", in *IEEE Conf. Rec.: 0-7803-7067-8/01, 2001, pp.1351-1356*

[6] R.Panda and R.K.Tripathi, "A symmetrical hybrid sine PWM switching technique for full bridge inverters", in India *International Conference on Power Electronics, 2006, 345-348.*

[7] A.Rodriguez, J., Lai, J. S. and Peng, F. Z. "Multilevel Inverter: A Survey of Topologies, Controls and Applications", *IEEE Trans. on Industrial Electronics, Vol. 49, No. 4 pp. 724-738 , 2000.*

[8] B.Shanthi and S.P.Natarajan, "Carrier overlapping PWM methods for single phase cascaded five level inverter", *International Journal of Science and Techniques of Automatic Control & Computer Engineering (IJ-STA, Tunisia), Special issue on Control of Electrical Machines,pp. 590-601, December 2008.*

[9] Urmila, B., and Subbarayudu, D., "Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques", *Journal of Scientific and Engineering Research*, vol.1, no.13, pp.1-5,2010.

[10] H. Wu, Y. Deng, Y. Liu, and X. He, "A New Clew For Research on PWM Methods of Multilevel Inverters: Principle and Applications," vol. 2, no. 1, 4-*12 IEEE Trans. Industry Applications, pp. 1251-1256, 2002.*