CDMA CODING TECHNIQUES FOR INTERCONNECT BETWEEN IP CORES

V.Ravichandran[1], Dr.G.K.D.Prasanna Venkatesan[2], R.Rani[3]

[1](ECE Department, M.I.E.T Engg College/ Anna University,Coimbatore, India)
[2](ECE Department, PGPCollege of Engg &Tech / Anna University,Coimbatore, India)
[3](Junior Telecom Officer(JTO),Mobile-VAS, BSNL, Tamil Nadu, India)

Abstract— *NoC(network On Chip) is an efficient approach to design the communication subsystem between IP Cores in SoC(System On Chip). In this paper a CDMA(code division multiple access)bus is proposed as a communication interconnect for different IP cores. CDMA has been proposed as an alternative way for interconnect of IP cores in a SoC design, or as a solution for interconnecting modules within a system realized in several PCBs. Compared to a conventional TDMA-based bus this paper present how a multiprocessor system can benefit from the use of concurrent data transfers.*
The simulation of the system using VHDL code is carried out. The performance of the system and is evaluated.

Keywords— *CDMA bus, Decoding, Encoding,NOC, Walshcode,*

I. INTRODUCTION:

A SoC consists of processing elements, I/O devices, Storage elements and integration structure linking all of them together. Processing elements could be processors that run embedded software or functional-specific hardware accelerators. As the number of processing elements increases, the interconnection plays an increasingly major role in system on-chip (SOC) design. The type of interconnection used for a specific application will heavily affect the performance and power consumption of the system. A variety of interconnection schemes is currently in use, including crossbars, rings, buses, and networks-on-chip. The shared-buses are among the most widely used communication architectures in systems-on-chip. The main advantages of shared-bus architectures include simple topology, low cost, and extensibility.

Several companies have developed their own on-chip bus architectures, such as Core-Connect, AMBA, and Silicon Micro-Networks. [12]

The main problem of shared-bus communications is that the performance of a bus decreases significantly when the bus size increases. This is the so-called scalability problem. Because a bus can be used by only one module at the time, the available bandwidth of one module decreases significantly as the bus size increases. The bandwidth can be improved by hierarchical bus architecture where multiple buses are connected with each other through bridges. However, hierarchical bus architectures may suffer from long communication latency for inter-bus communications.

1.1 Network-On Chip:

To overcome such problems, Research groups have started to investigate systematic approaches to the design of the communication part of SoCs. It turned out that the problem has to be addressed at all levels from the physical to the architectural to the operating system and application level.

Over the past few years, the idea of using networks-on-chip (NoCs) as viable on-chip communication fabrics for future multiprocessor systems-on-chips (MPSoCs) has been gaining traction. NoCs are an attempt to scale down the concepts of large scale networks, and apply them to the embedded system-on-chip (SoC) domain. Unlike traditional bus-based on-chip communication architectures, NoCs use packets to route data from the source to the destination component, via a network fabric that consists of switches (routers) and interconnection links (wires).

Hence, the term Network on Chip (NoC) is today used mostly in a very broad meaning, encompassing the hardware communication infra-structure, the middleware and operating system communication services and a design methodology and tools to map applications onto a NoC. All this together can be called a NoC platform. To overcome the above mentioned limitations, the attention has shifted towards the other popular interconnection architecture: network-on-chip (NOC). This communication scheme assumes that the data is packetized and then transmitted within a chip through a network.

The rest of this paper is arranged as follows. In Section II, we present Prior work related to Network on chip,Section III presents the motivation of the CDMA technique. The principle of CDMA NoC is presented in Section IV. A CDMA bus for onchip communication is presented in Section V. Experimental Result and analysis in Section VI.Finally,Section VII draws conclusion .

II. PRIOR WORKS:

2.1.On Chip interconnect mechanism

In general, on-chip communication architectures can be categorized into three main classes: Bus, point-to-point interconnects, and network-on-chip .However, there is no standard solution how to establish fast, flexible, efficient, and easy-to-design communication network to connect a large number of IP cores that have heterogeneous requirements[4]

In the figure we can observe the different types of on chip communication architectures. Fig.1.a shows Bus based architecture, Fig.1.b shows Point-to-point architecture and Fig.1.c shows Network on chip architecture.
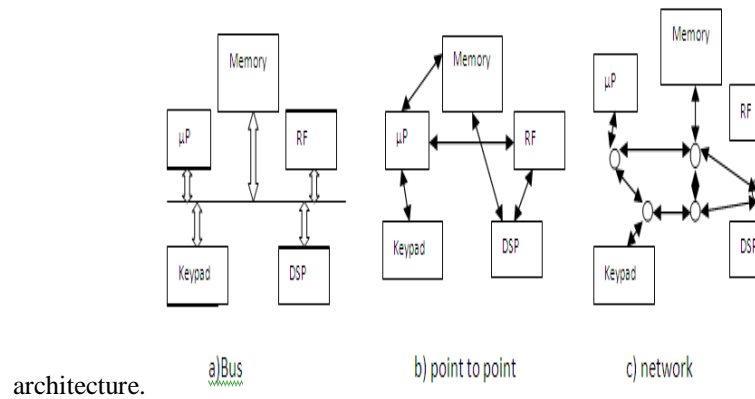
Fig.1 On chip Communication Architecture

2.2.TDMA based Interconnect

Most of interconnect networks in the SoC rely on parallel system bus, which apply time division multiple access, TDMA. The popularity and wide acceptance of the shared bus architecture is perhaps due to the fact that it is easy to adopt, well known among the computer industry, and also relatively inexpensive to implement. In those systems, the bus masters perform read and write operations with slave memory or I/O modules. However, bus-based architectures cannot scale up with an increasing number of components.

2.3.CDMA Based Interconnect

CDMA is a spread-spectrum technique that allows simultaneous use of the communication medium by multiple information links. It relies on the principle of codeword orthogonality, that avoids cross-correlation of code-words and allows perfect separation of information modulated with different code-words. Fig.2(a) shows the basic idea of CDMA based interconnect. Prior to transmitting the data onto the channel, each user modulates each transmitted bit with a spreading code.

The spreading code expands the transmission time from a single symbol into multiple chip periods. On the channel, multiple transmissions can coexist as a multi-level signal. At the receiver, this signal is correlated with the same spreading code that was applied at one of the transmitters. Because spreading codes are orthogonal, the original symbol that is transmitted by the transmitter can be retrieved.
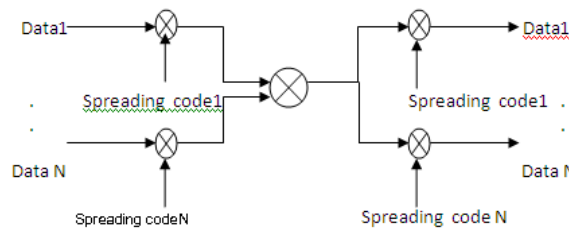
Fig.2.Principle of the CDMA technique

The Code Division Multiple Access, CDMA, is used to implement the memory/peripheral shared bus of multi-core systems consisting of multiple processing cores. In this method only bus lines that carry address and data signals are CDMA coded.

III.   MOTIVATION FOR USING CDMA TECHNIQUE

During realization of high speed buses we meet with numerous problems. These problems are typical for realization of a interconnection. To solve this problem various techniques are used. In most cases, these techniques include implementation of additional hardware. An alternative solution to increase bus throughput consists of increasing bus data transfer lines.

As a consequence, by using this approach, the number of lines, system complexity, occupied PCB area, and PCB tracing increase. In all cases, the buses with corresponding interfaces become very complex system. As a number of bus lines becomes higher the cost of these systems increases. Bearing this in mind, a bandwidth improvement achieved by increasing the number of bus lines, for most design solutions, is not a rational economical solution.

Compared to a conventional TDMA-based bus, a CDMA-based bus has better features concerning channel's isolation and channel's continuity in time domain since channels are divided by the spreading codes. CDMA technology relies on the principle of code word   orthogonally, such that it enables efficient separation of information [4] In our proposal, only bus lines that carry address and data signals are CDMA coded. The architecture of a multiprocessor system based on the CDMA shared bus is shown in Figure 2.

IV.   PRINCIPLE OF THE CDMA TECHNIQUE

4.1 CDMA Principle:

The principle of the CDMA technique is illustrated in Fig. 2.At the sending end, the data from different senders are encoded using a set of orthogonal spreading codes. The encoded data from different senders are added together for transmission without interfering with each other because of the orthogonal property of spreading codes. The orthogonal property means that the normalized autocorrelation value and the cross-correlation value of spreading codes are 1 and 0, respectively. Because of the orthogonal property, at the receiving end, the data can be decoded from the received sum signals by multiplying the received signals with the spreading code used for encoding[6].

In the encoding scheme data from different senders fed into the encoder bit by bit. Each data bit will be spread into S bits by XOR logic operations with a unique S-bit spreading code as illustrated in Fig. 3. Each bit of the S-bit encoded data generated by XOR operations is called a data chip. Then, the data chips which come from different senders are added together arithmetically according to their bit positions in the S-bit sequences. Namely, all the first data chips from different senders are added together and all the second data chips from different senders are added together, and so on.
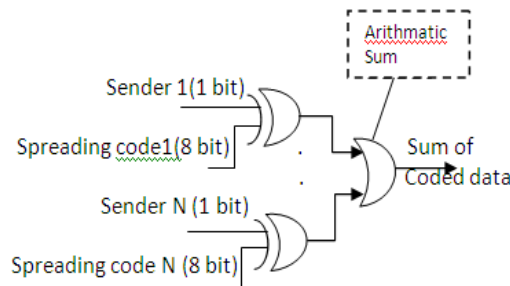
Fig.3. CDMA Encoding Scheme

Therefore, after the add operations, we will get S sum values of S-bit encoded data.
Then the binary equivalents of each sum value will be transferred to the receiving end. In this case, two binary bits are enough to represent the three possible different decimal sum values, "0," "1," and "2." For example, if a decimal sum value "2" needs to be transferred, we need to transfer two binary digits "10."

The decoding scheme can be explained as follows. If the original data bit to be transferred is "1," after the XOR operations in the encoding scheme illustrated in Fig. 3, it can only contribute nonzero value to the sums of data chips when a bit of spreading code is "0." Similarly, the 0-value original data bit can only contribute nonzero value to the sums o of data chips when a bit of spreading code is "1." Therefore, after accumulating the sum values according to the bit values of the spreading code, either the positive part or negative part is larger than the other if the spreading codes are orthogonal and balance. Hence, the original data bit can be decoded by comparing the values between the two accumulators. Namely, if the value of the positive accumulator is larger than the value in the negative accumulator, the original data bit is "1"; otherwise, the original data bit is "0."
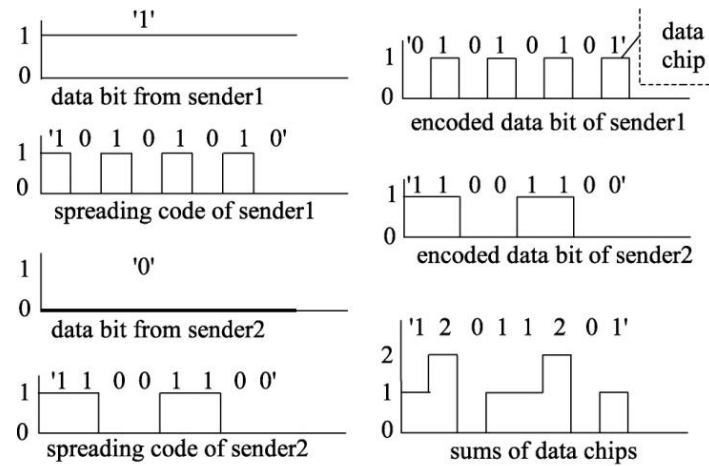
Fig.4.CDMA Encoding using Code words of Length 8

4.2 Spreading Code Selection

The proposed decoding scheme requires the spreading codes used in the CDMA NoC to have both the orthogonal and balance properties. Several types of spreading codes have been proposed for CDMA communication, such as Walsh code, M-sequence, Gold sequence, and Kasami sequence, etc. However, only Walsh code has the required orthogonal and balance properties. Therefore, Walsh code family is chosen as the spreading code library for the CDMA NoC.
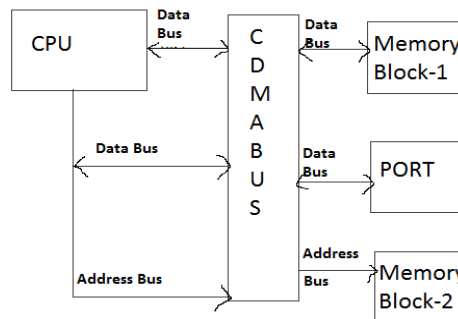
V.   CDMA BUS FOR ON CHIP COMMUNICATION

Fig.5 System Bus based on CDMA Technique

CDMA based bus system is used to connect peripherals like memory to CPU core. In this implementation a soft core processor, two memory blocks and one parallel port IP is integrated and connected by the designed CDMA bus. A 32 bit system bus is used to inter connect the peripherals with the CPU. The CDMA coded bus reduces the switching activities which implies the reduction of power consumption for on chip communication .This CDMA coded bus system is implemented on data bus and address bus.

VI.   EXPERIMENTAL RESULTS

The CDMA bus system is simulated using VHDL in MODELSIM software. the simulation and synthesis report says that CDMA based bus for peripheral communication is reliable one and low computation one ,by decreasing no lines for on chip peripheral communication it achieves low power consumption for bus based communication. In this work a 32 bit bus system is implemented for peripheral communication and communication is tested using sample data.

6.1.RESULT ANALYSIS

Results concerning datatransfer over CDMA bus analysed by simulation and synthesis report.Fig.2 shows the simulation result. From the synthesis report area and , latency for various device family are tabulated. Table No.1 shows the result for the encoder and in Table No-2 for the decoder.
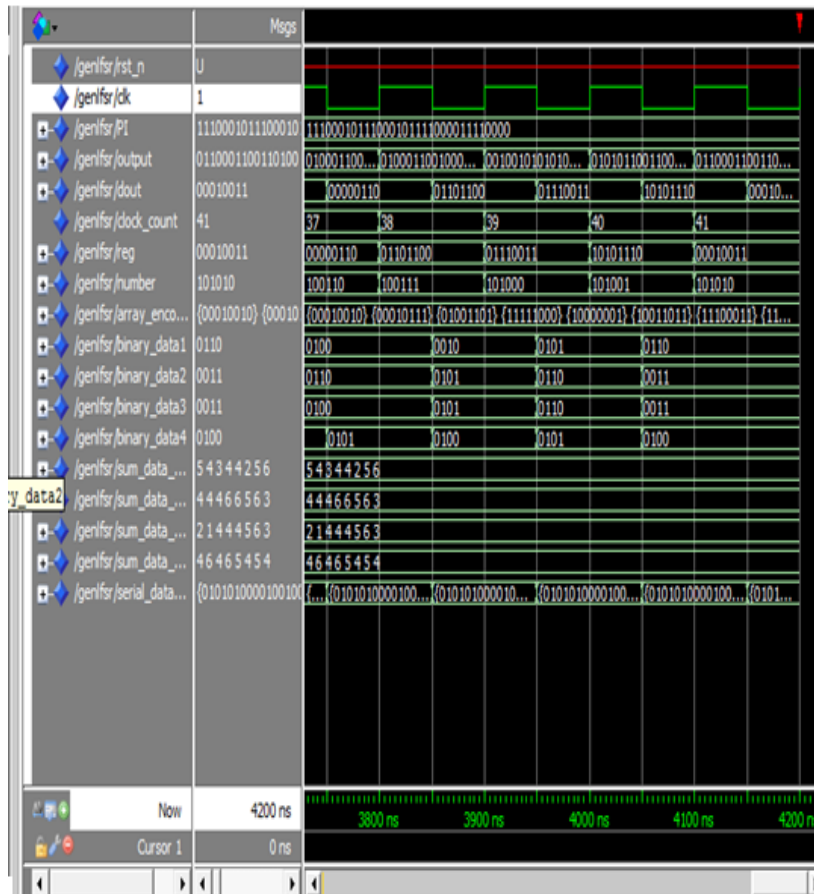
Fig.6 Simulation results of CDMA Scheme

6.2 Synthesis Report

Table.1 -CDMA Encoder performance

Device	Area(gate count)	latency
Spartan3E	810(84%)	3.056ns
Virtex4	810(13%)	1.586ns
Virtex5	276(1%)	1.257ns
VirtexE(XCV600E	869(12%)	3.820ns

6.3 .Resource utilisation Report

Table.2. CDMA decoder performance

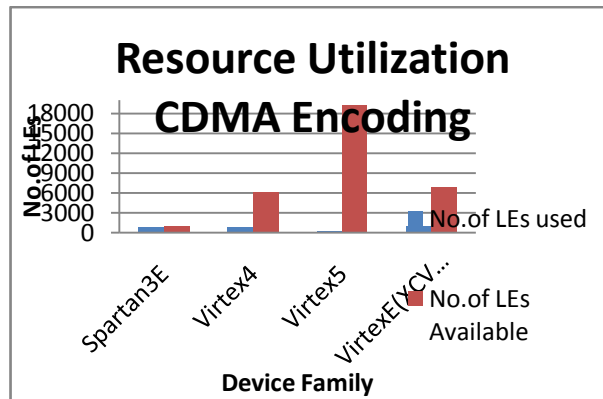| Device	Area(gate count)	latency
Spartan3E	237(24%)	19.612ns
Virtex4	233(3%)	10.685ns
Virtex5	67(1%)	8.446ns
VirtexE(XCV600E	256(33%)	21.394ns

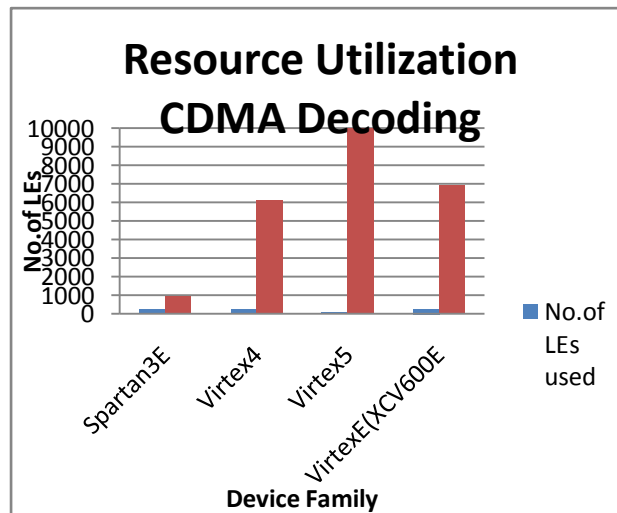**Fig.7.a. Resource Utilisation Performance of CDMA Encoding**

Fig.7.b. Resource Utilisation Performance of CDMA Decoding

The CDMA encoding and decoding was implemented in RTL level using VHDL.The simulation results of CDMA techniques as shown in fig(6).Resource utilization meant for utilization of LEs or ALUTs to the FPGA device family. In the performance graph, X-axis represent the device family and Y-axis represent the number of LEs or ALUTs used. The device families are Spartan 3E,Virtex 4,Virtex 5 and Virtex E(XCV600e) are chosen. Table.(1)&(2) shows comparison of device family with logical elements. From the above results, synthesis of CDMA Encoding using Spartan 3E family uses 810 LEs and decoding uses 237 Les out of 960 LEs available which is 84% and 24% respectively.Vertix5 family uses 276LEs and 67 LEs out of 19200 available which is 1% and 1% for encoding and decoding respectively. VertixE family uses 869 LEs and 256 LEs out of 6912 available which is 12% and 3% for encoding and decoding respectively.Vertix4 family uses 810 LEs and 233 LEs out of 6144 available which is 13% and 3% for encoding and decoding respectively. It shows that Vertix5 family has better resource utilization for both Encoding and Decoding.

VII. CONCLUSION

The CDMA based on chip communication system is simulated using VHDL in MODEL SIM software. The working of the system is verified by giving test vectors. The FPGA implementation resource utilization, area requirement, latency analysis are done for FPGA family of Spartan3E & Virtex.The best FPGA implementation family is found out thereby. From the above results we can conclude that the best implementation family is **Virtex5** due less area and latency. It is the Most advanced, high-performance,optimal-utilization compare with other family devices.

REFERENCES

[1] Tatjana Nikolic, Mile Stojcev, Goran Djordjevic "CDMA bus-based on-chip interconnect infrastructure",Elsevier 2009, pp.448-459.

[2] Vincenzo Rana,David Atienza,Macro Domenio santambrogio Donatella Scinto and Giovanni DeMicheli,"A Reconfigurable Networkonchip Architecture for optimal multiprocessor SOC communication" IFIP, VLSI-SOC 2010.PP.232-250.

[3] S. Pasricha and N. Dutt, "On-chip communication architectures: system on chip interconnect," Amsterdam: Elsevier Inc, 2008.

[4] S. Dey, K. Lahiri, and A. Raghunathan, "Design of communication architectures for high-performance and energy-efficient systems-onchips (in Multiprocessor Systems-on-Chips edited by A. Jerraya and W.Wolf)," San Francisco: Morgan Kaufman, 2005,pp.187-222

[5] M. Mitic, M. Stojcev, and Z. Stamenkovic, "An overview of SOC buses (in Digital   Systems and Applications edited by V. Oklobdzija)," Boca Raton: CRC Press, 2008.

[6] B. C. Lai, P. Schaumont, and I. Verbauwhede, "CT-bus: A heterogeneous   CDMA/TDMA bus for future SoC," Proc. 38th Annual Asilomar Conference on   Signals, Systems, and Computers, Monterey (CA) 2004,vol. 2, pp.1868-1872.

[7] J. Kim, I. Verbauwhede, and M.-C. F. Chang, "Design of an interconnect   architecture and signaling technology for parallelism in communication," IEEE   Transactions on Very Large Scale Integration (VLSI) Systems, 2007, vol. 15, pp.881–894.

[8] X. Wang, T. Ahonen, and J. Nurmi, "Applying CDMA technique to network-   on-chip," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, vol. 15,pp. 1091-1100.

[9] CoreConnect Bus Architecture, http://www.ibm.com/technology

[10] AMBA On-Chip Bus Standard, http://www.arm.com/armtech/AMBA

[11] K. Anjo, A. Okamura, and M. Motomura, "Wrapper-based bus implementation   techniques for performance improvement and cost reduction," IEEE Journal of   Solid- State Circuits, 2004, vol. 39, pp. 804-817.

[12] R. Lysecky and F. Vahid, "Pre-fetching for improved bus wrapper performance in cores," ACM Transaction on Design Automation of Electronic Systems, 2002, vol. 7, pp.58-90.

[13] K. L. Wu, J. M. Jou, and Y. H. Shiau, "Bus wrapper design methodology in   the SoC," Proc. 13th VLSI Design/CAD Symposium,Taitung   (Taiwan) 2002, pp. 524-527.

[14] T. Nikolic and M. Stojcev, "CDMA coded wrapper-based SoC interconnect,"   Proc. 43rd International Scientific Conference on information Communication, and Energy Systems and Technologies, Nis (Serbia) 2008,vol. 2, pp. 399-402.

[15] Innovations for High Performance microelectronics, http://www.ihpmicroelectronics.com

[16] Z. Stamenkovic and U. Jagdhold, "Digital Design Flow: A Case Study,"Proc. 45th Yugoslav ETRAN Conference, Arandjelovac (Serbia) 2001, pp. 74-77.

[17] Ching-Yuan Yang, Yu Lee, "A PWM and PAM Signaling Hybrid Technology   for Serial-Link Transceivers," IEEE Transactions on Instrumentation and Measurement, 2008,vol. 57,pp.1058-1070.

[18] D. J. Foley and M. P. Flynn, "A low-power 8-PAM serial transceiver in 0.5-μm digital CMOS," IEEE Journal of Solid-State Circuits, 2002, vol. 37, pp.310-316.

[19] K. S. Zigangirov, "Theory of Code Division Multiple Access Communication,"John Wiley & Sons, 2004.J. Wang, "Fundamentals of erbium-doped fiber amplifiers arrays (Periodical style—Submitted for publication)," *IEEE J. Quantum Electron.*, submitted for publication.

1. RAVICHANDRAN.V is a research scholar in the Elecronics and Communication at the Anna University Coimbatore,India.He received his B.E Degree in Electronics and Communication Engineering from MK University,Madurai,India.He received his M.E Degree in microwave and optical Engineering from M K Univrsity, Madurai,India. His reseach intrerests focused on on- chipnetworks and wireless communication.

2.Dr.G.K.D. PRASANNA VENKAESAN is received thePh. D., Information and Communication Engineering, from College of Engineering, Anna University, Chennai,India ,in 2006.He is a professor in the Department of Electronics and Communication Engineering. He Published   research papers more than 20 National and International Journals.He got 25 lakhs from AICTE ,under various funding schemes for research and development.His area of interest is WiMAX, WLAN, 3GPP and 3GPP2 standards

3. RANI.R is a Junior Telecom Officer(JTO),Mobile(VAS) in BSNL at the Trichy,Tamilnadu ,India.She received her B.E Degree in Electronics and Communication Engineering from Bharathithasan University,Trichy,India.She received her M.E Degree in Communication system from Anna University,Chennai,India. Her reseach intrerests focused on on- Optical and wireless communication.