Investigations on Three Phase Five Level Cascaded type FCMLI

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ABSTRACT

This work presents the comparison of various multicarrier based Pulse Width Modulation (PWM) techniques for the chosen H-bridge type Flying Capacitor Multi Level Inverter (FCMLI). In this paper, a H-bridge type FCMLI is controlled with Sinusoidal PWM (SPWM) technique with Phase Disposition (PD), Phase Opposition and Disposition (POD), Alternative Opposition and Disposition (APOD), Carrier Overlapping (CO), Phase Shift (PS) and Variable Frequency (VF) PWM techniques and the variation of Total Harmonic Distortion (THD) in the output is observed by varying the modulation index. Simulation is performed using MATLAB-SIMULINK. It is observed that sinusoidal reference with PSPWM provides output with relatively low distortion and relatively lower stress on the devices. It is also seen that COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices.

Keywords – APOD, CF, CO, FCMLI, PD, PS, POD, THD

I. INTRODUCTION

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. A group of semiconductor devices are connected in series to one single high voltage switch. Each group of such devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The research on the multilevel inverter technique now focuses on new multilevel topologies based on the existing multilevel topologies. The existing hybrid multilevel topologies utilize the Diode Clamped MultiLevel Inverter (DCMLI) or Flying Capacitor Multi Level Inverter (FCMLI) to replace the H-bridge as the basic module of the Modular Multi Level Inverter (MMLI) in order to reduce the number of the separate DC voltage sources. McGrath and Holmes [1] proposed a sinusoidal PWM of multilevel inverter in over modulation range. Lai and Peng [2] made a detailed survey on multilevel inverters. Corzine et al [3] described various control strategies for cascaded multilevel inverter. Haiwen et al [4] introduced hybrid cascaded multilevel inverter with PWM control method. Jing Zhao et al [5] developed a novel PWM control method for hybrid clamped multilevel inverters. Jinghua and Zhengxi [6] made a research on hybrid modulation strategies based on general hybrid topology of multilevel inverter. Govindaraju and Baskaran [7] proposed optimized hybrid phase disposition PWM control method for multilevel inverters. Zhong et al [8] developed fundamental frequency switching strategies of a seven level hybrid cascaded H-bridge multilevel inverter. Konstantinou et al [9] presented harmonic elimination control of a five level DC-AC cascaded H-bridge hybrid inverter.

Khoucha et al [10] introduced hybrid cascaded H-bridge multilevel inverter for induction motor drive applications. Sepahvand et al [11] presented a hybrid multilevel inverter with both staircase and PWM switching schemes. Satyanarayanan et al [12] developed hybrid algorithm based vector controlled induction motor drive to achieve superior waveform quality. This literature survey reveals few papers only on various FCMLI and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen H bridge type FCMLI employing sinusoidal switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

II. MULTILEVEL INVERTER

For research on multilevel inverter topologies, a preferred multilevel inverter topology shall have the following characteristics:
(i) The level is easy to extend
(ii) The number of the separate DC sources is few
iii) There is no voltage balance problem
iv) It has a modular structure
This paper presents a general multilevel hybrid topology through research on several basic multilevel topologies and introduces a few controllable degrees of freedom in the general hybrid topology. No matter what changes occur in the mentioned hybrid topologies, they can be resulted in change and combination of the degrees of freedom, which expand the topology collection of multilevel inverter. All the cascaded topologies are unified through introduction of the degrees of freedom in the general multilevel hybrid topology. Based on research on

hybrid topologies and multicarrier SPWM applied to multilevel inverter, the paper makes a deep study on various modulation strategies applied to hybrid topologies.

Fig. 1 shows a configuration of the three phase five level H bridge type FCMLI. The concept of this inverter is based on connecting H bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are $2n+1$ where n is the number of cells. The switching angles can be chosen in such a way that the THD is minimized. The output voltage obtained from FCMLI cascade is E/2. An n level cascaded H-bridge multilevel inverter needs $2(n$-$1)$ switching devices Similarly for FCMLI cascaded 2(n-1) switching devices are used. The gate signals for chosen five level cascaded type FCMLI are simulated using MATLAB-SIMULINK. The gate signal generator developed is tested for various values of modulation index m_a and for various PWM strategies. Fig.2 shows a sample SIMULINK developed for PDPWM technique. The simulation results presented in this paper in the form of the outputs of the chosen FCMLI cascaded are compared and evaluated.
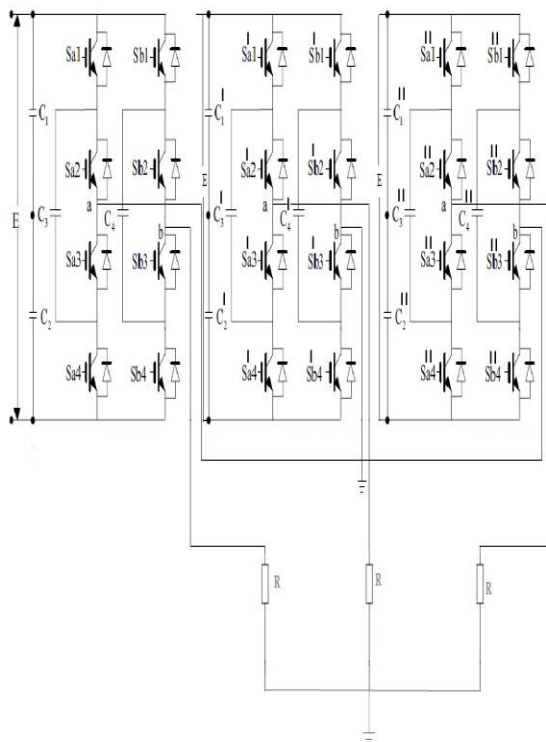

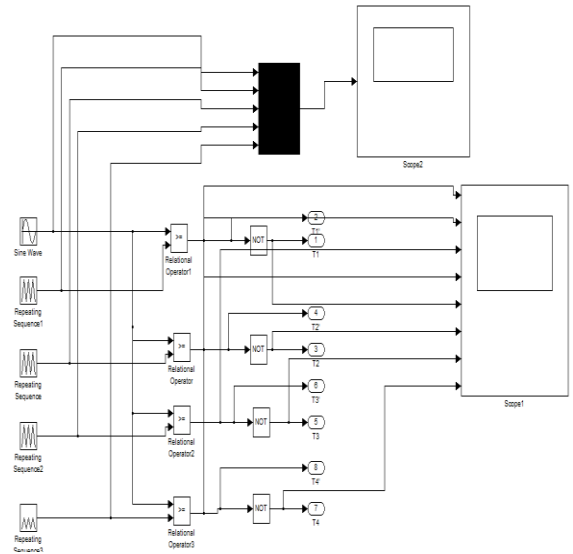Fig. 1 A three phase five level H-bridge type FCMLI

Fig. 2 Sample PWM generation logic using SIMULINK developed for PDPWM technique

III. MODULATION STRATEGIES

Development of concerns PWM control strategies the development of techniques to reduce the THD of the current. It is generally recognized that increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonics and associated sideband harmonics further away from the fundamental frequency component. The modulating/reference wave of multilevel carrier based PWM strategies can be sinusoidal. In general for a five level inverter four carriers are needed for symmetrical multilevel inverter. As far as the particular reference wave is concerned, there is also multiple Control Freedom Degree (CFD) including frequency, amplitude, phase angle of the reference wave. This paper focuses on hybrid power circuit with sinusoidal reference and triangular carrier which have been used in chosen three phase cascaded type FCMLI. The following strategies are employed in this study which have used the intersection of a sine wave with a triangular wave to generate firing pulses.

The amplitude modulation index for PD/POD/APOD/VFPWM = $2A_m/(m-1)A_c$.

The amplitude modulation index for PSPWM = $A_m / (A_c/2)$.

The amplitude modulation index for COPWM = $A_m/(m/4) A_C$.

$m_f = f_c/f_m$

where

f_c – Frequency of the carrier signal

f_m – Frequency of the reference signal

A_m –Amplitude of the reference signal

A_c – Amplitude of the carrier signal
m – number of levels.

III. (a) APOD strategy

As can be seen in the Fig.3 for a five level inverter a total of four carrier waves are used.

i) They are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees.

ii) The converter switches to + V_{dc} / 2 when the sine wave is higher than all carrier.

iii) The converter switches to +V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carrier.

iv) The converter switches to 0 when the sine wave is lower than the two uppermost carrier waveform and greater than two lowermost carrier.

v) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

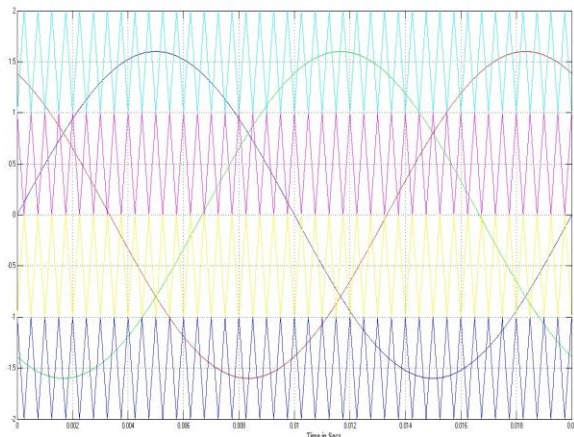vi) The converter switches to - V_{dc} / 2 when the sine wave is lesser than all carrier.

Fig. 3 Carrier arrangement for APODPWM strategy
(m_a = 0.8 and m_f = 40)

III. (b) POD strategy

a) Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180 degrees out of phase with those below zero.

b) The converter is switched to + V_{dc} / 2 when the sine wave is higher than both carrier waveforms.

c) The converter switches to +V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carrier.

d) The converter is switched to zero when the sine wave is greater than the lower carrier waveform but less than the upper carrier waveform.

e) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

f) The converter is switched to - V_{dc} / 2 when the sine wave is less than both carrier waveforms.

In the PWM scheme there are four triangles, upper two triangle have magnitude from 2 to 0 and the lower two triangles exist from 0 to –2 and these two triangle waveforms are out of phase.
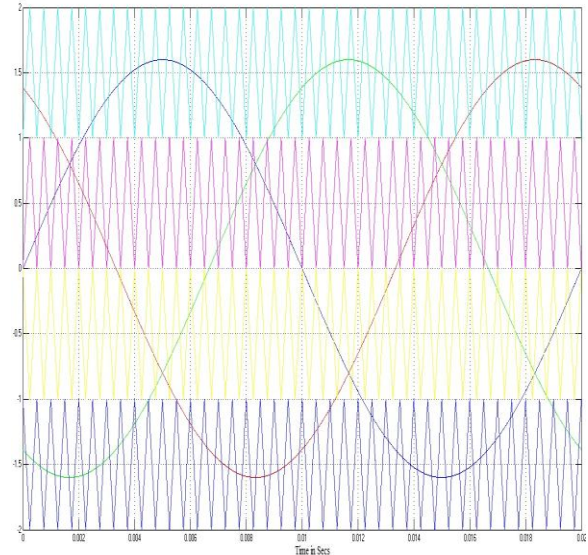

Fig. 4 Carrier arrangement for PODPWM strategy
(m_a = 0.8 and m_f = 40)

III. (c) PD strategy

The rules for phase disposition method for a multilevel inverter are

a) 4 carrier waveforms in phase are arranged.

b) The converter is switched to + V_{dc} / 2 when the sine wave is greater than both carriers.

c) The converter switches to +V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers.

d) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier .

e) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

f) The converter is switched to - V_{dc} / 2 when the sine wave is less than both carrier waveforms.

As can be seen from the Fig.5 in the PWM scheme there are four triangles, the upper two triangles ranges from 2 to 0 and the lower two triangle ranges from 0 to –2.
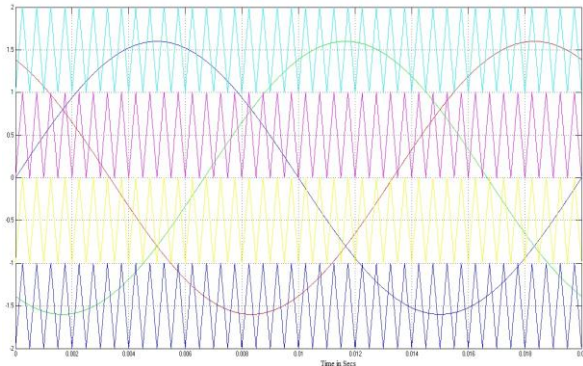
Fig. 5 Carrier arrangement for PDPWM strategy
($m_a = 0.8$ and $m_f = 40$)

III. (d) Carrier Overlapping (CO) strategy

For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_m and frequency of f_m and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off.
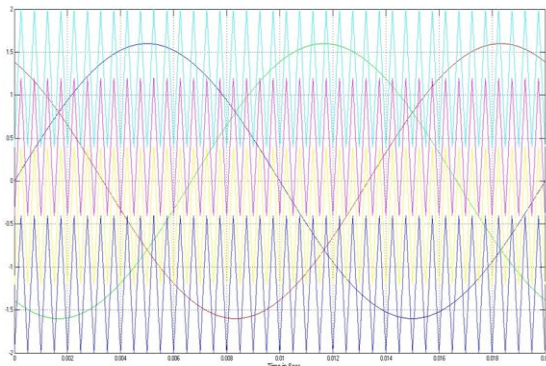

Fig. 6 Carrier arrangement for COPWM strategy
($m_a = 0.8$ and $m_f = 40$)

III. (e) VF strategy

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in PDPWM using constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in which the carrier frequency of the intermediate switches is

properly increased to balance the number of switchings for all the switches.
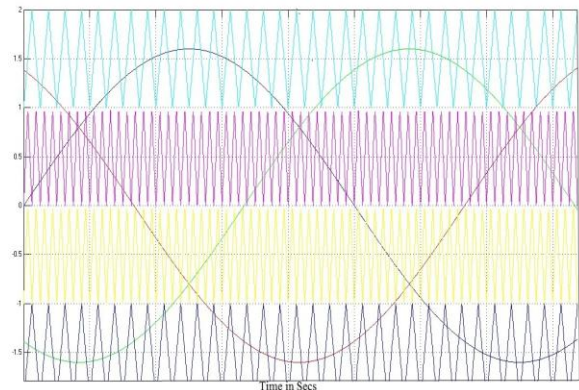

Fig. 7 Carrier arrangement for VFPWM strategy
($m_a = 0.8$ and $m_f = 40$)

III. (f) PS strategy

The phase shift multicarrier PWM technique uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltage.
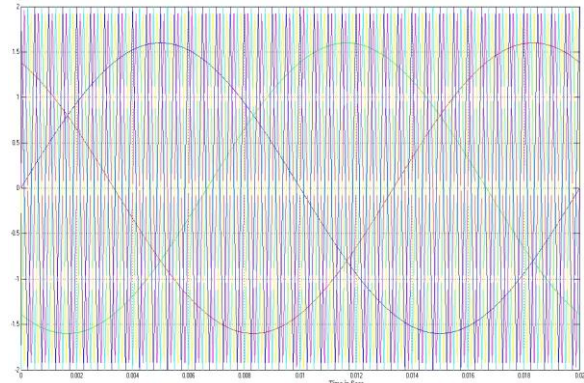

Fig.8 Carrier arrangement for PSPWM strategy
($m_a = 0.8$ and $m_f = 40$)

IV. SIMULATION RESULTS

The cascaded type FCMLI is modeled in SIMULINK using power system block set. Switching signals for FCMLI are developed using bipolar PWM techniques discussed previously. Simulation is performed for different values of m_a ranging from 0.6 – 1. The corresponding %THD values are measured using FFT block and they are shown in Table 1. Table 2 displays the V_{RMS} of fundamental of inverter output for same modulation indices. Figs 9-20 show the simulated output voltage of FCMLI and the corresponding FFT plots with above strategies but for only one sample value of $m_a = 0.8$. Fig.9 shows the five level output voltage generated by APOD strategy

and its FFT plot is shown in Fig.10. From Fig.10 it is observed that the APOD strategy produces significant 35th and 37th harmonic energy. Fig.11 shows the five level output voltage generated by POD strategy and its FFT plot is shown in Fig.12. From Fig.12 it is observed that the POD produces significant 33rd and 35th harmonic energy. Fig.13 shows the five level output voltage generated by PD strategy and its FFT plot is shown in Fig.14. From Fig.14 it is observed that the PD strategy produces significant 30th, 32nd, 36th and 38th harmonic energy. Fig.15 shows the five level output voltage generated by CO strategy and its FFT plot is shown in Fig.16. From Fig.16 it is observed that the CO strategy produces significant 3rd and 38th harmonic energy.

Fig.17 shows the five level output voltage generated by VF strategy and its FFT plot is shown in Fig.18. From Fig.18 it is observed that the VF strategy produces significant 34th and 38th harmonic energy. Fig.19 shows the five level output voltage generated by PS strategy and its FFT plot is shown in Fig.20. From Fig.20 it is observed that the PS strategy does not produce significant harmonic energy. The following parameter values are used for simulation: V_{DC} =440V, f_c = 2KHz and R (load) = 100 ohms.
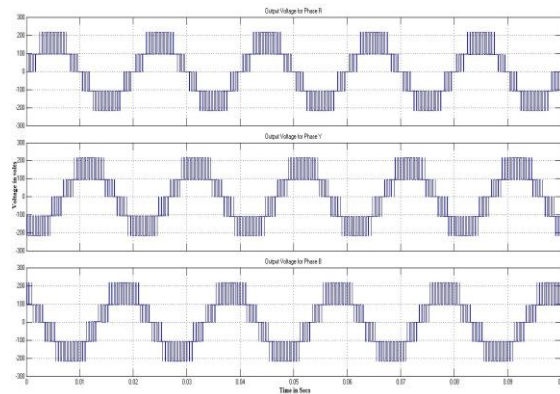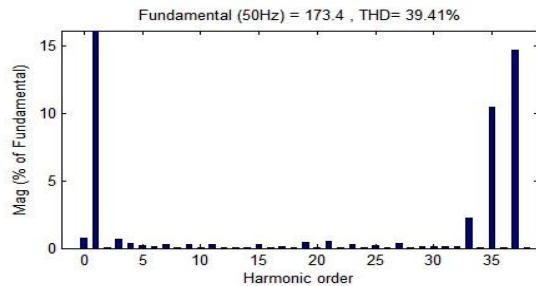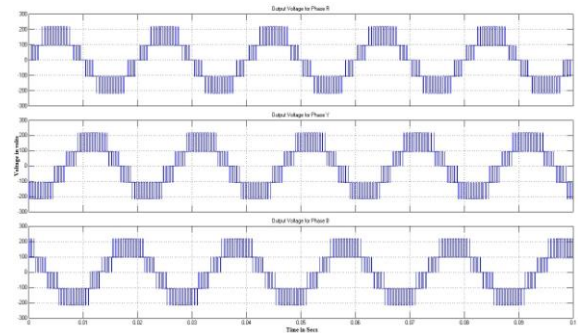

Fig.11 Output voltage generated by PODPWM strategy

Fig.12 FFT plot for output voltage of PODPWM strategy
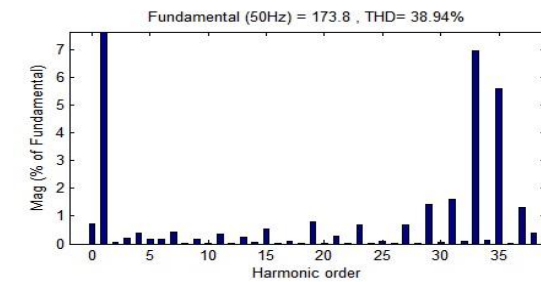

Fig.9 Output voltage generated by APODPWM strategy

Fig.13 Output voltage generated by PDPWM strategy

Fig.10 FFT plot for output voltage of APODPWM strategy

Fig.14 FFT plot for output voltage of PDPWM strategy

Fig.15 Output voltage generated by COPWM strategy
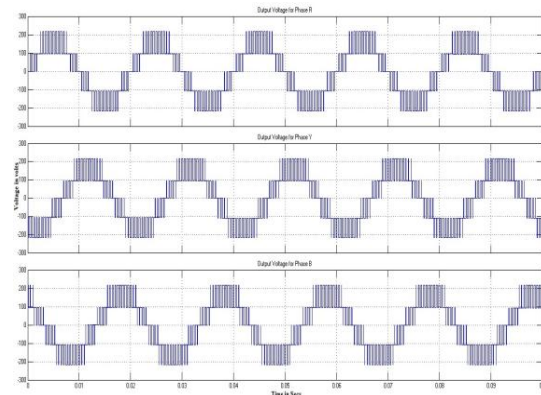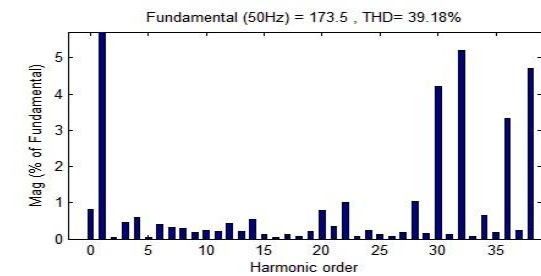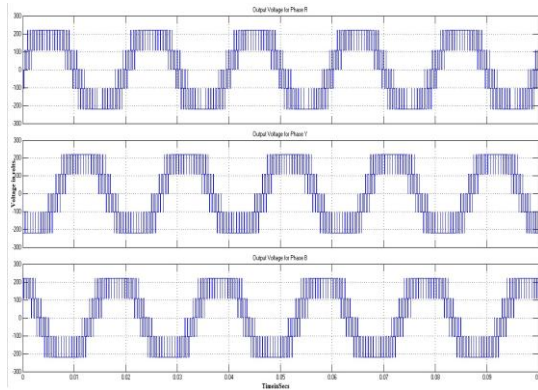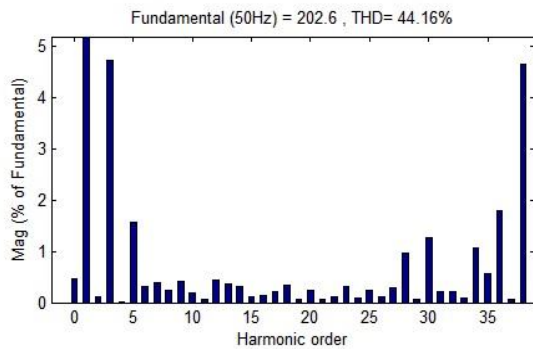
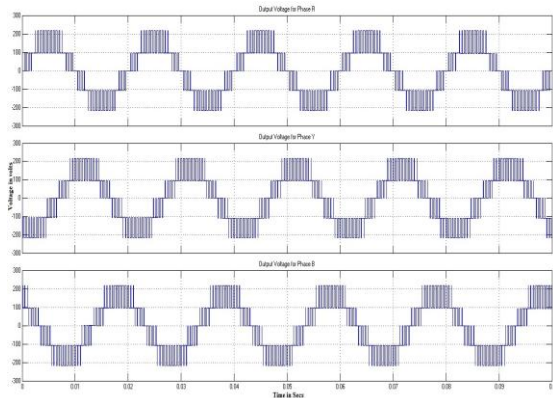

Fig.18 FFT plot for output voltage of VFPWM strategy

Fig.16 FFT plot for output voltage of COPWM strategy
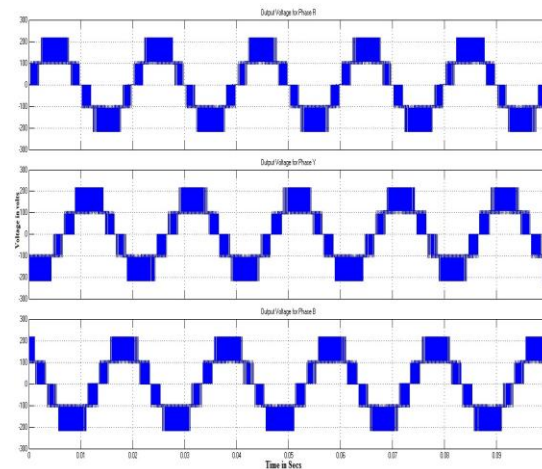
Fig.19 Output voltage generated by PSPWM strategy

Fig.17 Output voltage generated by VFPWM strategy
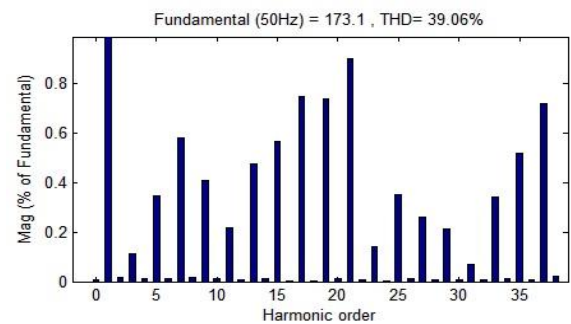
Fig.20 FFT plot for output voltage of PSPWM strategy

Table-1 % THD for different modulation indices

m_a	PD	POD	APOD	CO	VF	PS
1	27.41	27.33	27.92	32.31	27.44	27.55
0.9	34.24	34.14	34.65	38.84	34.1	33.42
0.8	39.18	38.94	39.41	44.16	39.13	39.06
0.7	42.9	42.71	42.97	55.44	43.31	42.22
0.6	45.02	45.07	44.95	66.62	45.06	44.91

Table-2 V_{RMS} (fundamental) for different modulation indices

m_a	PD	POD	APOD	CO	VF	PS
1	154.4	154.4	154.2	157.8	154.4	154.5
0.9	138.6	138.6	138.4	144	138.6	138.8
0.8	122.7	122.9	122.6	**128.9**	122.8	122.4
0.7	106.7	106.5	106.7	110.5	106.4	107.1
0.6	90.86	90.66	90.91	91.01	91.06	90.11

Table-3 Crest factor for different modulation indices

m_a	PD	POD	APOD	CO	VF	PS
1	1.41386	1.41386	1.414397	1.414449	1.415155	1.412945
0.9	1.414141	1.414141	1.414017	1.414583	1.415584	1.412104
0.8	1.414018	1.414158	1.414356	1.571761	1.409609	1.418301
0.7	1.413308	1.415023	1.414246	1.413575	1.422932	1.405229
0.6	1.414264	1.414075	1.414586	1.41413	1.399078	1.429364

Table-4 Form factor for different modulation indices

m_a	PD	POD	APOD	CO	VF	PS
1	199.32	175.5	174.47	10.24	28343.42	140.61
0.9	150.76	128.09	127.44	7.44	11433.27	151.49
0.8	86.71	98.08	98.15	6.42	12578.35	111.94
0.7	105.74	77.11	76.54	4.07	11028.73	87.35
0.6	75.9	61.92	61.71	2.99	11576.31	64.12

V. CONCLUSION

It is observed from Table 1 PSPWM technique provides output with relatively low distortion. COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage (Table 2) and also relatively lower stress on the devices. Table 3 shows crest factor. Next table 4 provides FF for all modulation indices.

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