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Design of Low Power, Low Voltage Multiplier for Wide Applications

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ABSTRACT
Analog multipliers found its wide spread applications in the era of signal processing, neural networks as well as frequency doublers, RMS circuits and phase detectors (phase lock loop). The major advantages of multiplier are high speed, low power high linearity, and less dc offset error. This paper presents how multipliers are used in such applications. Supply voltage is 0.5V. The circuits are designed and simulated using TSPICE simulator by level 49 parameters (TSMC) in 0.8 um standard CMOS technology.

Keywords- **Four-Quadrant Multiplier, Frequency Multipliers, Phase Lock-Loop.**

1. INTRODUCTION
Analog multiplier is an important basic building block in communication systems like analog signal processing systems; for example frequency mixers, variable gain amplifiers, adaptive filters, phase-locked loop, amplitude modulators, frequency doublers, rectifiers and demodulators etc. A multiplier performs the linear product of two signals either in current domain or voltage domain. When both the input signals are free to take either of positive or negative polarity then the multiplier is said to perform four quadrant multiplications. Since multiplication is performed by nonlinear devices (BJT, MOSFET) so the linear range in which multiplier can yield expected output is limited according to the topology of circuits. The basic block diagram of four-quadrant voltage mode Multiplier is shown in Figure 1. The purpose of implementation of this multiplier is to implement applications of multiplier.

2. SCHEMATIC OF FOUR-QUADRANT MULTIPLIER
Here we present a low voltage, low power, high linearity and high speed Multiplier circuit which operates in the voltage mode using parallel connected MOS devices at the input side and diode connected MOS devices as a load at the output side. Figure 12

shows how transistors can be used to implement Multipliers. In order to reduce the number of devices parallel structure is useful compared to cascaded structure. The basic block diagram of four- quadrant voltage mode Multiplier is shown in Figure 1. The purpose of implementing this structure is to reduce the number of devices with minimum size. In this design, instead of using NMOS at the load side PMOS are used because of its negative threshold voltage.

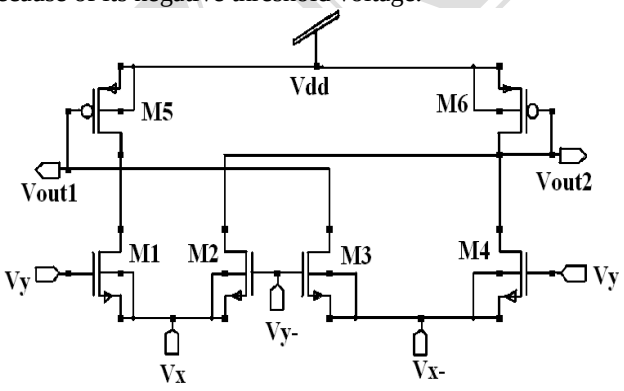


Fig. 1 Four Quadrant Multiplier

Since transistors are operating in the triode region, let us consider the equation for small signal model.[4]

$$i_d = K' V_{ds} V_{gs} \quad (1)$$

$$V_{ds_1} = V_{0_1} - V_x \quad (2)$$

$$V_{ds_2} = V_{0_2} - V_x \quad (3)$$

$$V_{ds_3} = V_{0_1} + V_x \quad (4)$$

$$V_{ds_4} = V_{0_2} + V_x \quad (5)$$

$$i_{d_1} = K' V_{ds_1} (V_x - V_y) \quad (6)$$

$$i_{d_2} = K' V_{ds_2} (-V_y - V_x) \quad (7)$$

$$i_{d_3} = K' V_{ds_3} (-V_y + V_x) \quad (8)$$

$$i_{d_4} = K' V_{ds_4} (V_y + V_x) \quad (9)$$

$$i_{d_1} + i_{d_3} = K' \left[\left(-2V_x V_y \right) + \left(2V_x^2 \right) \right] \quad (10)$$

$$i_{d_2} + i_{d_4} = K'\left[(2V_xV_y) + (2V_x^2)\right] \quad (11)$$

$$(i_{d_2} + i_{d_4}) - (i_{d_1} + i_{d_3}) = 4K'V_xV_y \quad (12)$$

Above equation shows that the output of Multiplier is depends on the transconductance parameter, which in turn depends on the threshold voltage and W/L ratio of the device.

3. SIMULATION RESULTS

Output of the Multiplier is differential output and is as shown in Figure 3 i.e. $V_{out} = (V_{o1} - V_{02})$ and is obtained by setting $V_{x1} = V_{x2}$ =1GHz and $V_{y1} = V_{y2}$ =10GHz. Input signals are shown in Figure 2. Common mode noise gets eliminated completely because of differential output.

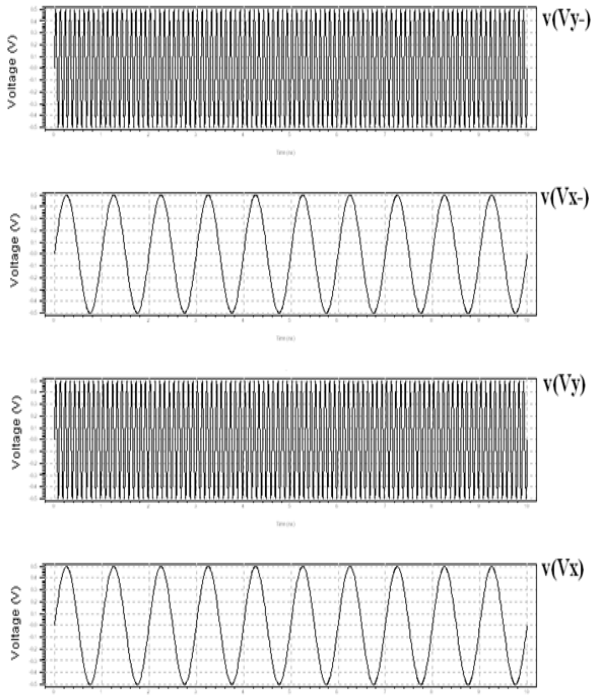


Fig. 2 Inputs to the Multiplier

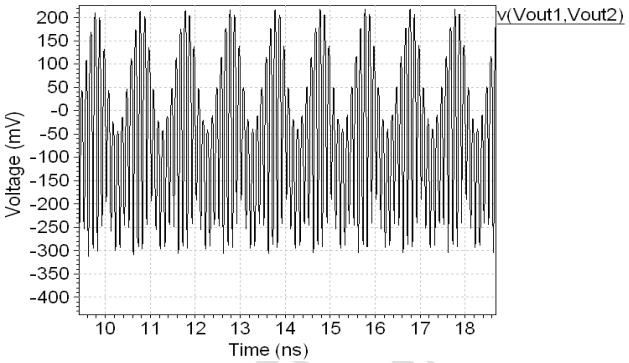


Fig. 3 Outputs of the Multiplier

4. APPLICATIONS OF MULTIPLIERS

There are many applications of multipliers. Few of them are given below. All these are designed by introducing four-quadrant multiplier.

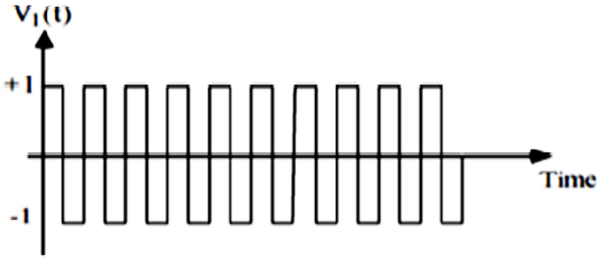
4.1. Modulators

Modulator a process where an information-carrying signal is introduced into a carrier signal. In amplitude Modulation, the amplitude of the carrier carries the information of the modulating signal

$$V_o = V_{cA}(1 + mcos\omega_c t)cos\omega_c t$$

$$= V_1V_2cos\omega_c t + \frac{V_1V_2}{2}mcos(\omega_c - \omega_m)t + \frac{V_1V_2}{2}cos(\omega_c + \omega_m)t \quad (13)$$

For higher frequencies, single device modulators are used and the square-law term of the transfer characteristics of the device provides the multiplication function which is done by MOS device not by BJT.



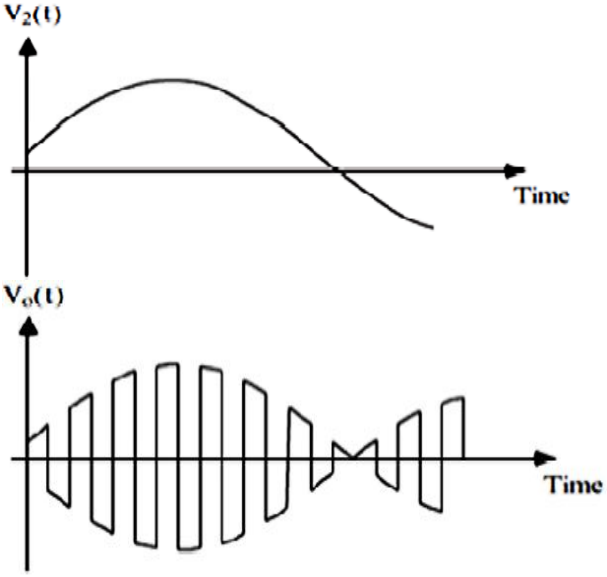


Fig. 4 Amplitude Modulation

$$V_o(t) = K\big(V_c(t)V_m(t)\big)$$
$$= K\sum_{n=1}^{\infty} V_1V_2\cos nW_ct + V_1V_2 cosW_mt$$
$$= \sum_{n=1}^{\omega} V_1V_2\cos(nW_ct - W_nt) + V_1V_2\cos(nW_ct + W_nt) \quad (14)$$

4.2. Phase Locked-Loop

Phase detector is an essential element in phase locked loops. PLL's are widely used in frequency synthesizer. Phase lock loop is universal building block used in both analog and digital applications. The basic structure of phase lock loop is shown in figure . Phase detector finds the phase difference between input and output signals of the controlled oscillator and locks the PLL on zero phase difference. Analog multiplier is most widely used as phase detector in PLL's.

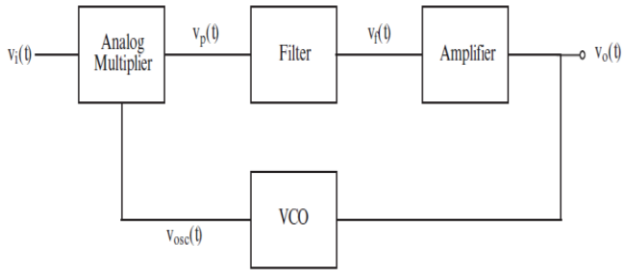


Fig. 5 Block diagram of a phase lock loop

If unmodulated signals of identical frequency are applied to the inputs, the circuit behaves as a phase detector and produces an output whose dc component is proportional to the phase difference between the two inputs.the output waveform that results is shown in figure and consist of a dc component at twice the incoming frequency .the dc component is given by

$$V_{avg} = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)d(W_ot) \quad (15)$$

If input signals are comparable to or smaller than V_t, the circuit still act as a phase detector. However the output voltage then depend both on the phase difference and on the amplitude of the two input waveforms.

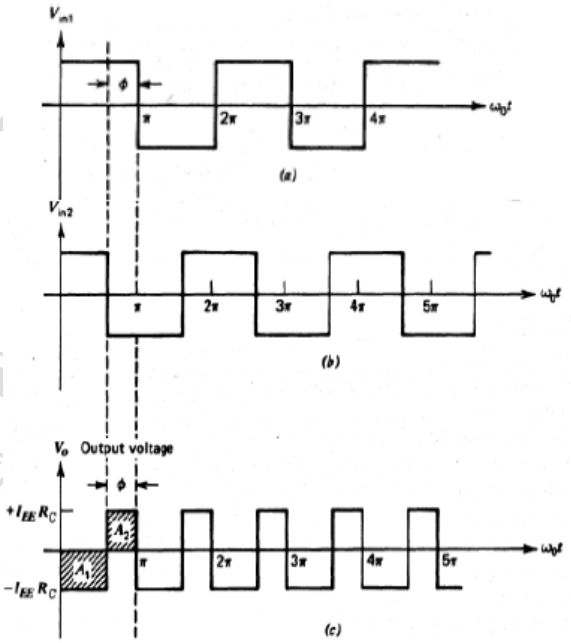


Fig. 6 (a) signal 1(b) signal 2 (c) Phase detector output

4.3. Generation of integer powers

By connect the two input of a multiplier together, a square can be obtained. If the input to the square can be

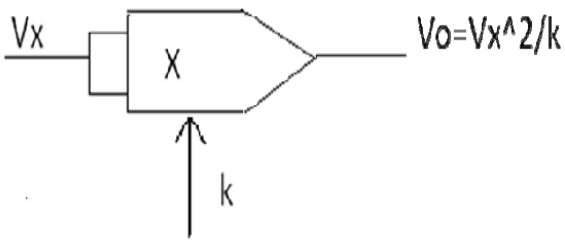


Fig. 7 Squarer

obtained. If input to the square is V_x, the output is $\frac{V^2}{2K}$. By feeding the output of square along with original input to another multiplier, we get a squarer. The same principle can be extended to generate any higher integer power of analog signals.

4.4. Frequency Multiplier

A square can be used as a frequency doubler. If the input V_x to the squarer is sinusoidal signal, a sin ωt, its output is given as

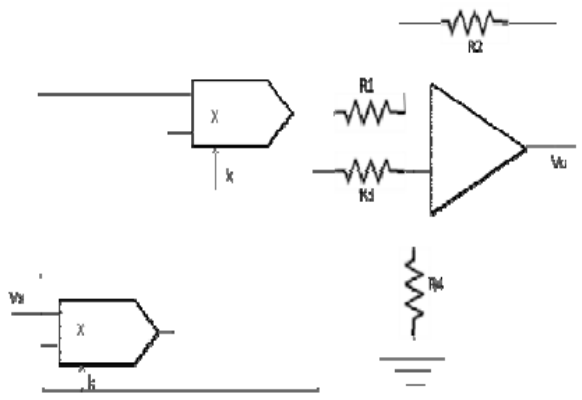


Fig. 8 Frequency Tripler

$$V_o = \frac{A^2 sin^2(\omega t)}{k} \quad (16)$$

$$= \frac{A^2(1-\cos(2\omega t))}{k} \quad (17)$$

Thus the output signal contains the dc component and co sinusoidal component of frequency 2ω, which is twice that of input signal.

5. CONCLUSION

In this paper "Low Power, Low Voltage High Speed Multiplier with Applications", the multiplier circuit is implemented in 180nm technology with minimum transistor sizes (W/L=180nm/180nm). It can be operated even at low Supply voltage VDD=0.5V. Band width of operation is about 4THz, which is suitable for high frequency/high speed applications. This circuit has very less THD. Therefore the proposed structure with less number of transistors occupies less area and hence consumes less power. In this paper applications of multiplier are given to analyze further implementations. The circuit is designed using 180nm-TSMC MOSIS Level- 49 model and then simulated using TSPICE (SPICE Simulator). Major issue of this paper is to design a low power, low voltage, high speed multiplier with less area along with its applications.

TABLE I. PARAMETER TABLE

Parameters	Multiplier
W/L(minimum)	180nm/180nm
VDD	o.5 V
Offset error across output	Zero Volt
Linearity error	Less compared to GHz Multiplier
Power in watts	700Uw
Vx and-Vx	500mV,1GHz
Vy and-Vy	500mV,10GHz
No. of transistors	6

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