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INVESTIGATION OF DIGITAL CONTROL STRATEGY FOR ASYMMETRIC CASCADED MULTILEVEL INVERTER

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Abstract-The cascaded multilevel inverter (CMLI) has gained much attention in recent years due to its advantages in high voltage and high power with low harmonics applications [1]. A standard cascaded multilevel inverter requires n DC sources for 2n+1 levels at the output, where n is the number of inverter stages. This paper presents a topology to control cascaded multilevel inverter that is implemented with multiple DC sources to get 2^{n+1}- 1 levels [2]. Without using Pulse Width Modulation (PWM) technique, the firing circuit can be implemented using flip-flop which greatly reduces the Total Harmonic Distortion (THD) and switching losses. To develop the model of a cascaded hybrid multilevel inverter, a simulation is done based on MATLAB/SIMULINK software. Their integration makes the design and analysis of a hybrid multilevel inverter more complete and detailed.

Keywords- Multilevel inverter, Cascaded inverter, Digital control, Total Harmonic distortion, Switching losses.

I.INTRODUCTION

The concept of cascaded multilevel inverter has gained popularity in recent years that entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility and higher voltage capability [3-4].However, the main disadvantages of multilevel inverter include unbalance voltage difficulties, unequal current stresses and higher implementation cost. Several topologies for multilevel inverters have been proposed in the literature, the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different DC sources on the individual H- bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters [5].

This paper presents multilevel inverter consisting of series connection of separate single (full bridge) or three phase inverter modules or cells on the ac output terminals. This topology is suitable for applications where separate DC voltage sources are available, such as photovoltaic (pv) generators, fuel cells and batteries. To implement cascaded multilevel inverter firing sequence is required, which in turn needs n+2 bit counter. Section II deals with the basic operation of asymmetric cascaded multilevel inverter. Section III discusses about the digital control technique. Section IV focuses on the simulation results using MATLAB. Section V deals with the conclusions.

II.ASYMMETRIC CASCADED MULTILEVEL INVERTER

The cascaded H-bridges inverter consists of H-bridges in series configuration. Such technology is very attractive for application such as [6-7] motor drive systems, power distribution, power quality and power conditioning application. Each H-bridge inverter module can generate three different output voltage levels namely 0, $+V_{dc}$ and $-V_{dc}$. The multilevel inverter of Fig.1 utilizes two independent DC sources and consequently will create an output phase voltage with seven levels. N is the number of independent DC sources per phase, m is the number of levels, l represents the number of switches with freewheeling diodes per phase, then the following equations are applied for CMLI :

$$m = 2N + 1 \quad (1)$$

$$l = 2(m - 1) \quad (2)$$

A simplified single phase topology is shown in Fig. 1 The output voltage will be +10V (top inverter H_1) when switches T_{11} and T_{14} conducts. Similarly -10V will be obtained when T_{12} and T_{13} conducts. The output voltage is +20V only when T_{21} and T_{24} are conducting and the output voltage is -20V only when T_{22} and T_{23} are conducting. The output voltage +30V is available when switches T_{11} ,T_{14} ,T_{21} and T_{24} conducts and -30V is available when switches T_{12},T_{13} T_{22} and T_{23} conducts.

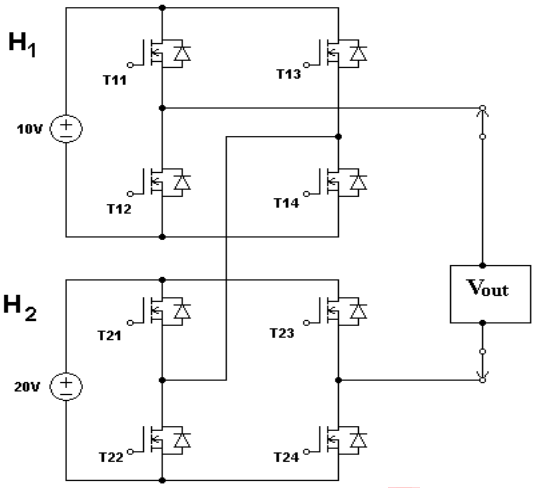

Fig.1 Power circuit of CMLI

Table1. TRUTH TABLE FOR TRIGERRING SWITCHES

Voltage	T_{11}	T_{12}	T_{13}	T_{14}	T_{21}	T_{22}	T_{23}	T_{24}
-30	0	1	1	0	0	1	1	0
-20	0	0	0	0	0	1	1	0
-10	0	1	1	0	0	0	0	0
0	1	1	1	1	0	0	0	0
10	1	0	0	1	0	0	0	0
20	0	0	0	0	1	0	0	1
30	1	0	0	1	1	0	0	1

III.DIGITAL CONTROL TECHNIQUE

The output bits of flip-flop1 are represented as Q1 and $\overline{Q1}$. Similarly for filp-flop2 to flip-flop4 the output bits are represented as Q2 &$\overline{Q2}$, Q3 &$\overline{Q3}$, Q4 &$\overline{Q4}$. For seven-level inverter we need n+2 bit counters. The counter is operated in conventional manner so that it acts as up counter. The output of flip-flop1 (Q1) and flip-flop2 (Q2) are made to operate forward for first half of the positive cycle and in reverse for the second half of the positive cycle. Similarly they are operated for negative cycle. The modification of bits Q1 and Q2 are done using bits Q4 and $\overline{Q3}$. For the first half of the positive or negative cycle the count has to increase so as to increase the output voltage in steps and this is done by bit Q3'. For the remaining positive or negative half cycle the count has to decrement and the voltage descend in steps and this is done by bit Q3. The pulse separation is needed to separate positive and negative cycle and this is done with the help of bits Q4 and $\overline{Q4}$ and these bits are used as control bits in the circuit. This proposed method of multi level inverter consists of DC sources such as 10V and 20V which are scaled in terms of multiples of two. Fig. shows the firing circuit. MATLAB software does not support counter operation directly so it is implemented using J-K flip-flop. The flip-flop output is given to AND and OR gates to generate six different gating pattern for multilevel inverter. The output of logic gates is in the form of Boolean and logical conversion of Boolean to double is done using data conversion block. This is because IGBT accept signals in the form of double for its gate.

The firing circuit is divided into three sections namely counter stage, logic circuit and pulse separation. The counter operates as up counter and counts from 0000 to 1111. The bits Q3 and Q4 are used as control bits for the logic circuit and pulse separation. Fig.3 shows the output of firing circuit (out1 to out6) are given to various gates of power switches. The gating patterns of various switches are shown in Fig.4a to Fig.4f.

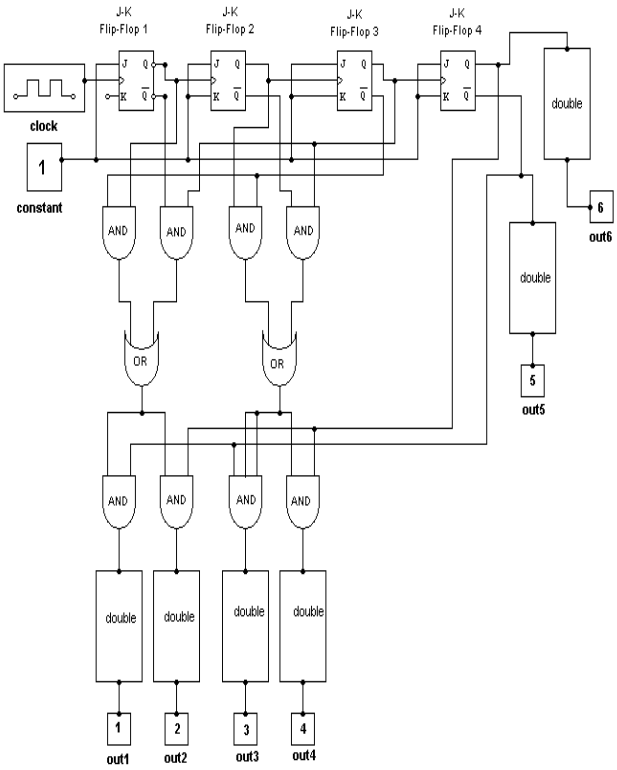

Fig.2 Firing circuit

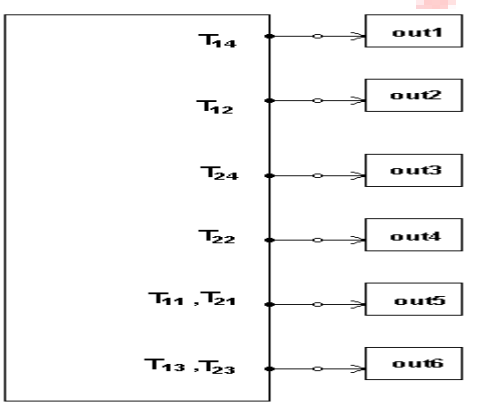

Fig.3 Firing unit

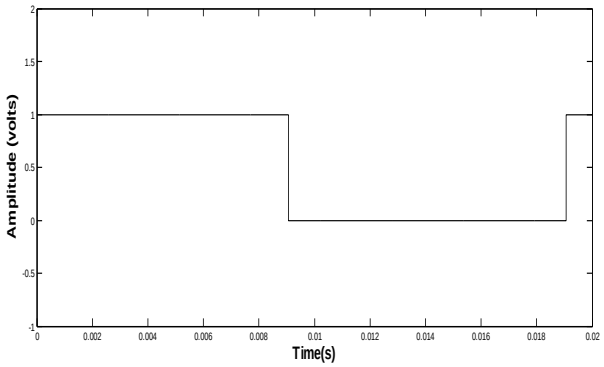

Fig.4a.Gating pattern of Switches (T_{11} , T_{21})

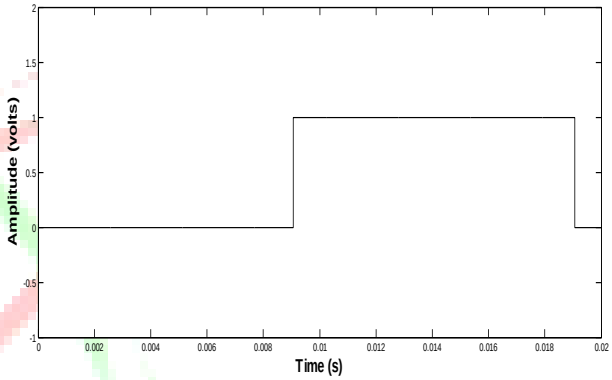

Fig.4b.Gating pattern of Switch (T_{13}, T_{23})

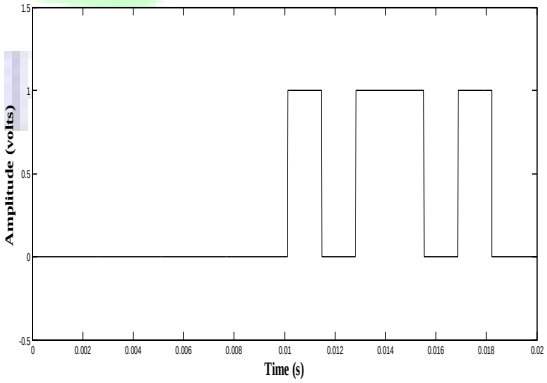

Fig.4c.Gating pattern of Switch (T_{12})

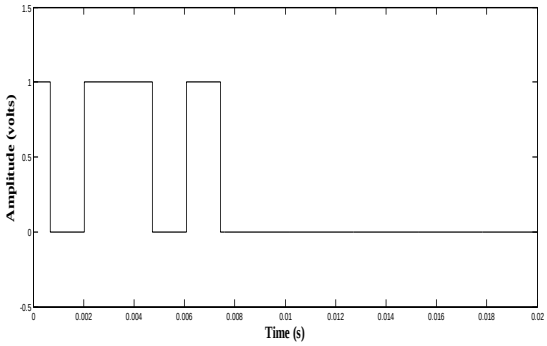

Fig.4d.Gating pattern of Switch (T_{14})

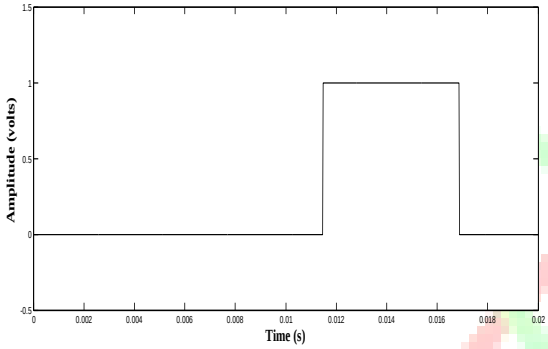

Fig.4e.Gating pattern of Switch (T_{22})

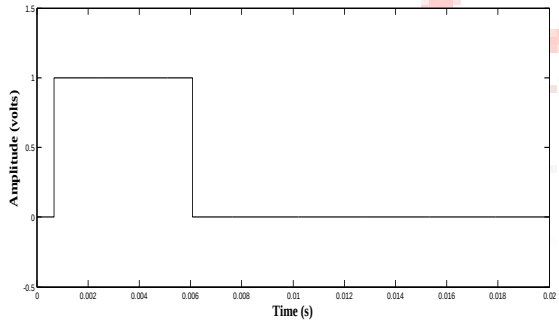

Fig.4f.Gating pattern of Switch (T_{24})

IV.SIMULATION RESULTS

Staircase modulation technique have been proposed using non integer dc source voltage ratios for multilevel inverter to achieve mimimum total harmonic distortion (THD)[8-9]. MATLAB/Simulink is used to create the simulation model as shown. The individual inverter outputs and seven level output are shown in Fig.5a,5b and 5c.The Fast Fourier Transform (FFT) analysis of the load voltage waveform of the proposed inverter is shown in Fig.5d. Fig.6 shows the graph between Switching Frequency Vs Total Harmonic Distortion (THD) [10].

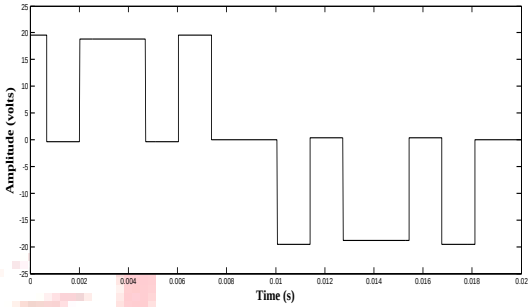

Fig.5a Output of Inverter 1.

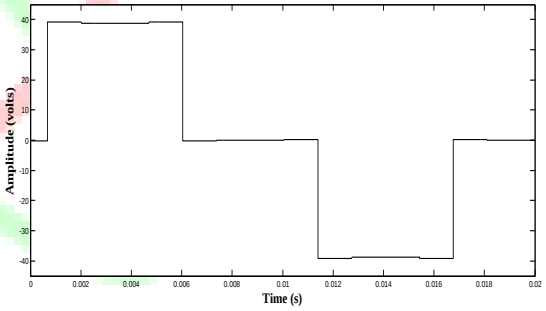

Fig.5b Output of Inverter 2.

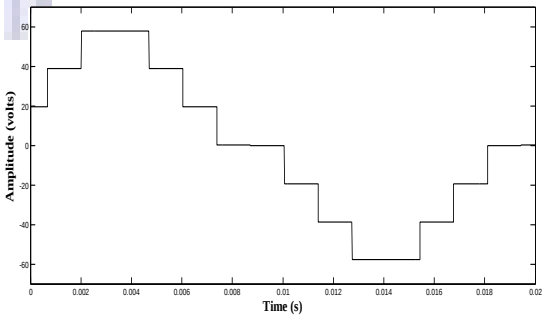

Fig.5c Seven level output of inverter

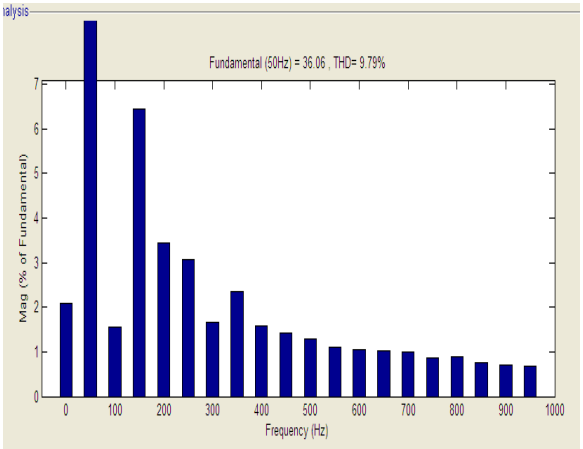

Fig.5d FFT analysis of load voltage for seven- level inverter

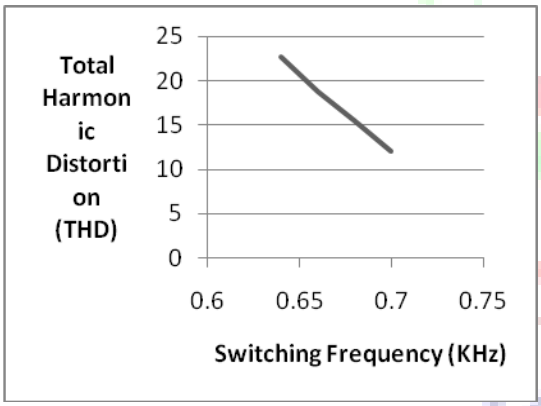

Fig.6 Switching Frequency Vs THD

V. EXPERIMENTAL RESULTS

Two H- Bridge inverters are formed using MOSFETs and they are cascaded to obtain a seven level output voltage. To implement the cascaded seven-level inverter in an effective way, transformers, bridge rectifiers and voltage regulators are used to form 12V DC supply for opto-couplers. Opto-couplers form the driver circuit for MOSFETs. The output from driver circuits is given across the gate and source of the MOSFETs and the prototype of the multilevel inverter is shown in Fig.7.

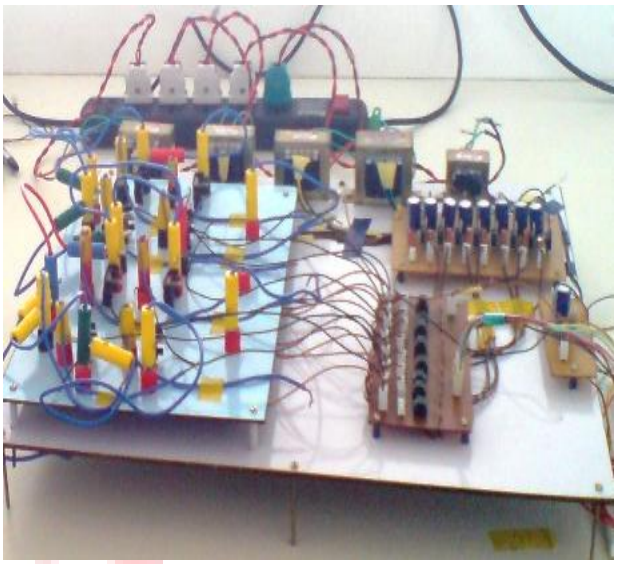

Fig.7. Photograph of the prototype of seven-level inverter

The experimental load voltage waveform for the seven-level asymmetric inverter employing digital control technique is shown in Fig.8.

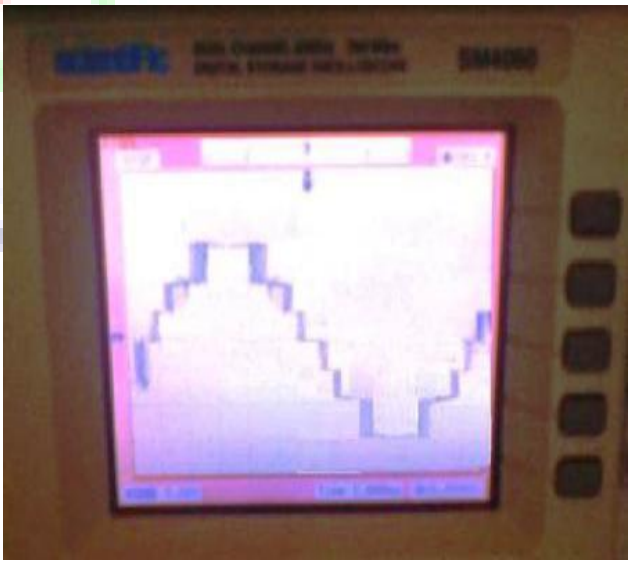

Fig.8 Experimental load voltage waveform of seven-level inverter

VI.CONCLUSION

In this paper digital switching scheme is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches, switching losses when compared to the conventional multilevel inverter using PWM technique[11] and harmonics are reduced using the increased steps in the output voltage. From the FFT analysis we get minimum THD of 9.79% and the value can be still reduced by increasing the number of stages [12]. Consequently, the system efficiency can be improved. This proposed system eliminates the complexity of generating gate signals when the stages are added. The simulation results show that this hybrid multilevel inverter topology can be applied for high power applications.

VI.REFERENCES

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BIOGRAPHY

Dr.R.Seyezhai obtained her B.E. (Electronics & Communication Engineering) from Noorul Islam College of Engineering, Nagercoil in 1996 and her M.E in Power Electronics & Drives from Shanmugha College of Engineering, Thanjavur in 1998 and Ph.D from Anna University, Chennai, in 2010 . She has been working in the teaching field for about 13 Years. She has published 85 papers in the area of Power Electronics & Drives. Her areas of interest include SiC Power Devices & Multilevel Inverters.