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# Clock Control Based Timing Error Tolerant System

**Darsi Madhavi[1], Bandi Dinesh Kumar Reddy[2], E.C.Gokul[3], S.Deva Kumar[4], S.Babitha[5], T.Guna Sekhar[6]**

*Assistant Professor[1] ,Department Of Electronics And Communication Engineering , Siddharth Institute Of Engineering And Technology, Puttur, AP , India-517583*
*Student[2,3,4,5,6] ,ECE Department, Siddharth Institute Of Engineering And Technology, AP , India-517583*
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**ABSTRACT:**
During recent years, due to the technological advancements the increasing rate of mistake occurrence on semiconductors, timing error is currently receiving more attention. Because the latest semiconductor operates at a high frequency and with a low supply voltage, even little external disturbances can jeopardize the timing margin between successive clocks. Many strategies have been introduced to cope with a timing mistake. Existing approaches to alleviate a timing fault, on the other hand, are primarily focused on time-delaying mechanisms and overly complex operations, resulting in a timing problem on clock-based systems as well as hardware overhead. To address this, we offer a timing-error-tolerant technique that uses a simple mechanism to instantaneously fix a timing issue. The proposed technique can recover a timing error without losing time in a clock-based system by altering a clock in a flip-flop
**Key Words:** Pulsed Latch, Error Tolerant System, Transition Detector,Time Borrowing Circuit, Error Signal, Master Clock Generator.

## I. INTRODUCTION

Timing errors are an increasing reliability concern in nanometer technology, high complexity, and multi-voltage\frequency integrated circuits. Process variability in device and circuit parameters is one of the primary challenges currently faced by the semiconductor industry. Besides static variations that occur during chip fabrication, dynamic parameter variation – resulting from environmental and workload changes – is also possible during the chip's operation. With the 0.4-V operation, the logical path with the worst case is 12x slower than that with the typical case With increasing process and environmental variations in deep-sub micrometer technologies, meeting performance specifications with a limited power budget becomes a critical challenge. The traditional worst-case corner-based design introduces a "safety margin" to tolerate variations. The timing error occurs because of the delay in combinational circuits that are located between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly. To deal with the timing error, many related methods have been proposed.

This paper presents a method to prevent the timing errors in advance to improve tolerance to delay variations in logic stages in a pipelined system with a minimized performance penalty (less than a clock cycle) while operating the system at a clock period less than the critical path delay. The optimization of transparency windows of pulsed latches can achieve the minimum power-delay product of pipelines. To avoid the penalty of the clock, time-borrowing methods have been introduced. Since it corrects a timing error by borrowing time from the next pipeline stage, the whole system is not delayed in the recovery of a timing error. It consists of two master latches and one slave latch to correct a timing error.

## II. EXISTING APPROACH

The "pulsed latch" technology is used in today's error-tolerant systems. A pulsed latch has time-borrowing properties, which relaxes the timing requirement. The pulsed latch can sample the proper data due to this time-borrowing behavior as long as the path delay is smaller than the total of the clock period and time-borrowing window. However, the borrowed time is added to the next stage's path delay. If the increased path delay is larger than the total of the clock period and time-borrowing window in the next stage, the pulsed latch in that stage will be unable to sample the proper data. As a result, the number of errors in each stage increases, causing a data delay.

In this technology, the entire system, including the error correcting system, is controlled by a single clock. As a result, anytime the pulsing latch borrows the clock, the clock of the entire system changes, creating an abrupt behavior for a brief amount of time, resulting in increased power consumption for a brief period.

## III. PROPOSED METHODOLOGY

In this article, we propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. We use a Time borrowing Circuit In the critical path, the abnormal data transition after the rising edge of the clock, which is caused by a timing error, is detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing method that copes with the successive errors is introduced as shown in the block diagram below

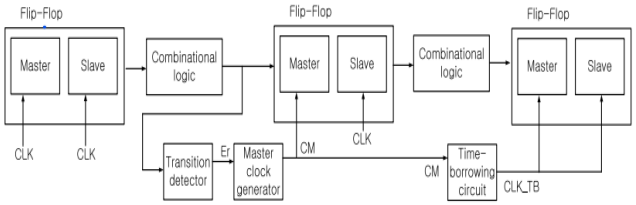



**Figure1.Block Diagram of proposed system**

The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing method that copes with the successive errors is introduced. If the timing error occurs in two stages successively, modified CLK in the second stage maintains a transparent window for enough time to make normal data be stored without changing the system CLK. From Figure1 we can observe that two clocks are being used they are CLK(System clock) and CLK_TB(Time borrowed clock).

The internal circuits of the transition detector, Master Clock Generator, and time borrowing circuits are shown below.

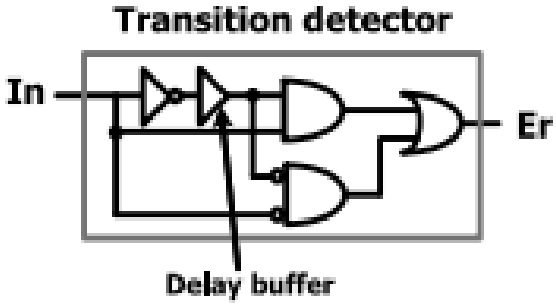
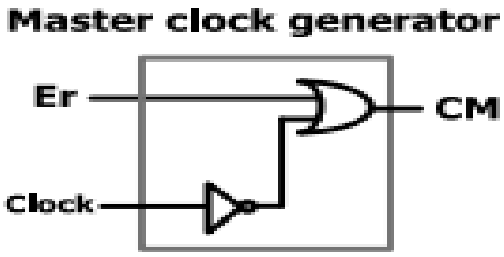



**Figure2. Internal Circuit of Transition Detector**




**Figurre3. Internal circuit of Master clock generator**

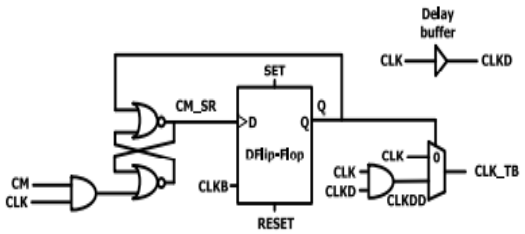



**Figure4. Internal circuit of time borrowing system**

A CM (Clock of Master) is high for a certain time after a timing error occurs. Hence the delayed data can be stored as normal data. The time-borrowing scheme can be used in any location that has a short setup time for the flip-flop.

## IV. ADVANTAGES

This particular System has following advantages:

[1] No need of additional clock for error recovery due to controlling action of clock signal.
[2] Error detects and corrects instantly.
[3] Low Area overhead as it consists of less no. of logics.
[4] Avoid of clock penalty for time borrower circuit.

## V. FUTURE SCOPE

This can be further improved under the following circumstances

1. Improving the technology that is used in designing the circuit (less than 45nm)
2. Using enhanced time management techniques in order to reduce the delay
3. Reducing the number of transistors used to reduce power consumption

## VI. RESULTS

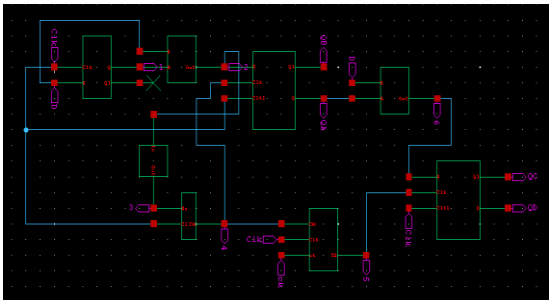


**Figure 23: Schematic Circuit of Proposed system using Time Borrow Technique.**

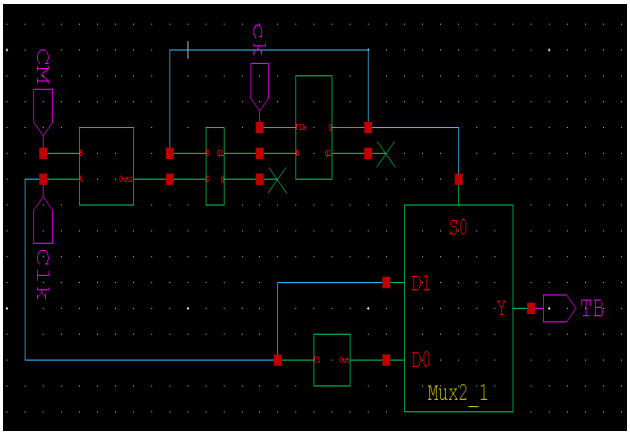



**Figure 24: Schematic of Time Borrow circuit.**

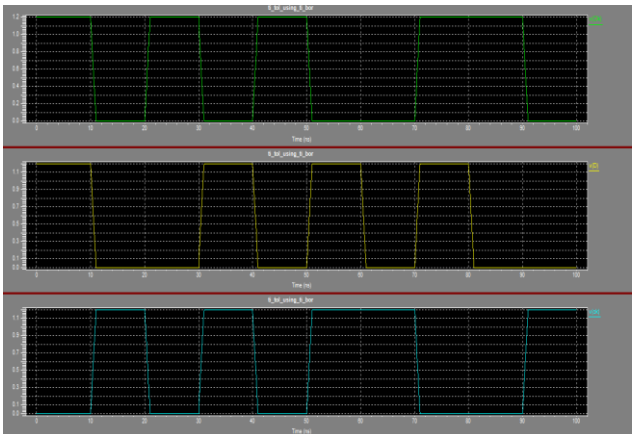
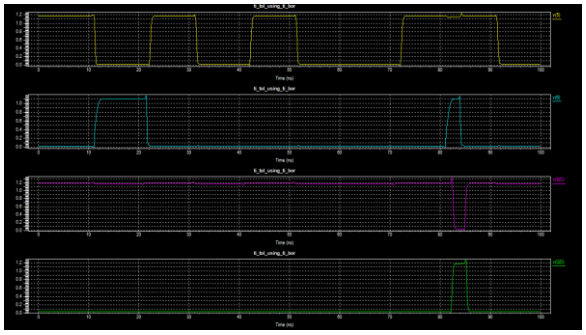


**Figure 25: Inputs for the proposed system with Time Borrow Technique.**



**proposed system with Time borrow circuit**

## VII. CONCLUSION

Through this project we can present an effective method to detect and correct timing errors using Timing error-tolerant circuit using Time borrowing technique. In the critical path, the abnormal data transition after the edge of the clock can be detected and corrected by controlling the transparent window of the clock.

The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing technique that deals with the successive-stage error is introduced. If the timing error occurs in the second stage successively, modified CLK maintains the transparent window during enough period of time for timing-error tolerance without changing system CLK.

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