IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 10, Issue 2, February 2020, ||Series -I|| PP 07-15

Review of Power Minimization Techniques in Transition Fault Testing

S. Asha Pon,[a]V. Jeyalakshmi[b]
[a]Research Scholar,[b]Professor
[a,b]Depatrment of ECE, College of Engineering, Guindy, Tamil Nadu, India
Received 20 January 2020; Accepted 10 February 2020

Abstract: Low power testing is a breakthrough in the modern integrated design world. Digital devices embedded with BIST are designed to work in normal and test mode. Increased activation of embedded architectures and application of large number of test patterns during testing leads to excess power consumption during test mode. Increase in power consumption during testing damages the packages, Circuit Under Test (CUT) and also reliability of the devices. The survey briefs the need for low power transition testing, the concept of transition fault testing and describes existing techniques to minimize power during transition fault testing. The intent of the survey is to identify and develop an efficient power minimization technique with highest fault coverage.
Keywords: ATPG; LOC; LOS; Scan path organization; Test vector ordering; Transition fault testing

I. INTRODUCTION

Testing of digital devices is an important and challenging task. Based on the survey, it is clear that testing with external test equipment faces drawbacks such as [1]:

i. high cost of the tester
ii. consume moretime to generate and apply test patterns to CUT
iii. external tester faces difficulty to test large circuits, due to the handling of huge volume of test pattern

The drawbacks can be effectively overcome by Built in Self Techniques (BIST)[2]. Digital devices embedded with BIST are designed to work in normal and test mode. Power consumption of digital devices are high in test mode than normal mode of operation[3].

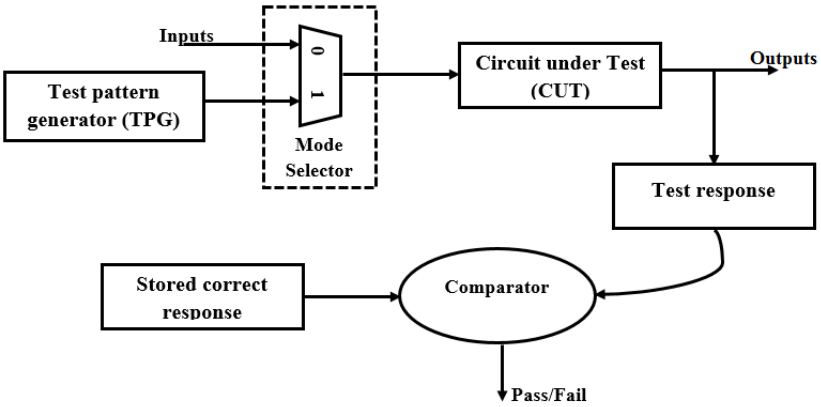

Fig. 1. Built-In Self-Test

Fig. 1. Briefs the concept of BIST. Mode selector plays the role of selection. At normal mode, inputs are fed to the CUT and the outputs are obtained. Under, test mode of operation, CUT is supplied with the test patterns from pattern generator. Obtained test responses are compared against the stored correct responses by the comparator. Comparator decides whether CUT passes or fails the test, based on comparison result.

Delay testing is of a great challenge to today's IC industries. Decreased clock rate and increased number of transistors, causesvaried kinds of defect in the circuit, henceforth, delaying the output and making it to exceed the total clock interval. This defect leads to the delay fault and it can be modelled [4] as given in Fig. 2.

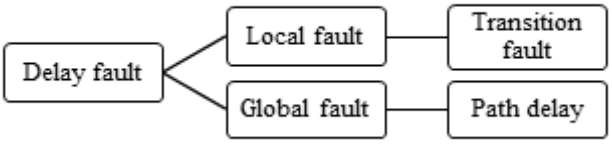

Fig. 2. Flow chart – Delay fault

Fault at a particular node is termed as local fault and the fault along a path is termed as global fault. An increased delay to a gate makes the time interval of the propagated output to exceed the clock interval which is termed as transition fault. Path delay is the aggregation of delay in a path through which the output is propagated.

Power supply noise affects the path and transition delay testing by delaying the target paths during test mode of operation. Hence attention of DFT engineers are driven towards methodological development to reduce power supply noise [5]. The power supply noise is high during at-speed scan testing, due to the usage of larger test patterns at higher clock frequencies than functional operation.

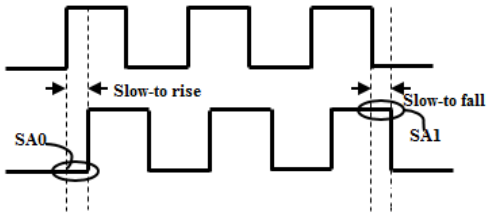

Fig. 3. Transition fault

Transition fault is meant to locate delay defects in a single location and increased delay due to signal transition by using two vectors, namely, initialization vector V_1 and propagation vector V_2. Rise and fall time of the signal increases due to the presence of delay during signal transition, leading to the occurrence of slow-to-rise and slow-to-fall transition faults [5, 6]. Transition fault can be modelled by stuck-at fault simulator, because, during slow-to-rise, the signal line is temporarily stuck to logic '0', stuck-at 0 (SA0) and on slow-to-fall, signal line is temporarily stuck to logic '1', stuck-at 1 (SA1) as illustrated in Fig. 3.

The existing schemes namely, Launch-off-shift (LOS) and Launch-off-capture (LOC) are used to generate test patterns for transition fault. As shown in Fig. 4.second vector V2-10110 is the one bit shift of first vector V1-01101 for launch-off-shift or skewed-load [7]. V2 is the response of combinational part and V1 is the scanned in vector for the launch-off-capture orbroadside transition testing [8] as shown in Fig. 5.

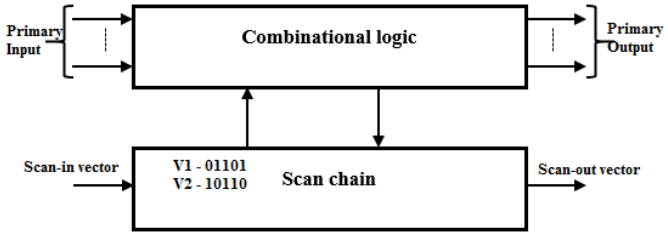

Fig. 4. LOS scheme

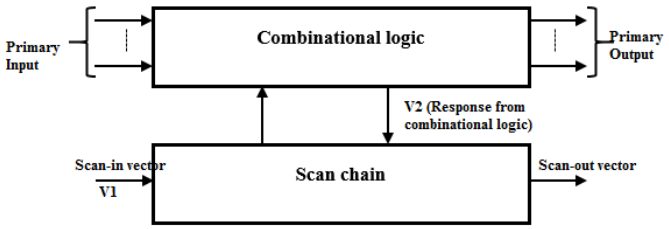

Fig.5. LOC scheme

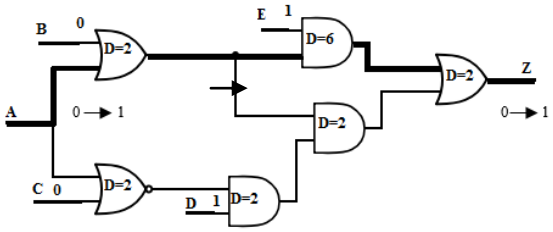

Fig. 6. Transition fault model

Fig. 6. displays a model of combinational circuit with transition fault. Logic gates in the circuit are provided with certain delay values. An initialization vector V_1 = 00011 is provided and a transition is initiated at node A (0 1), now, the propagation vector is V_2 = 10011. Due to the extra delay at node A the transition is propagated to the primary output Z after 12ns, which is larger than the total gate delay (10 ns). The transition fault is the measure of time difference between the vector V_1 and V_2.

Fig. 7 and Fig. 8 illustrate the output waveform generated for the example given in Fig. 6. As shown in Fig. 7 the resultant output is obtained at 10ns, because the total delay along the longest path is 10. When a signal transition is initiated at node A with an additional delay of 2ns, the transition at the output node Z can be viewed after 12ns as mentioned in Fig. 8. This indicates the presence of transition fault at node A due to the additional delay.

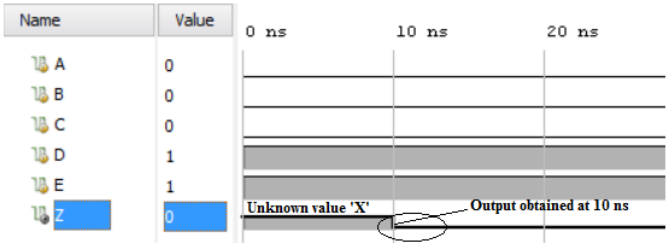

Fig. 7. Output without fault

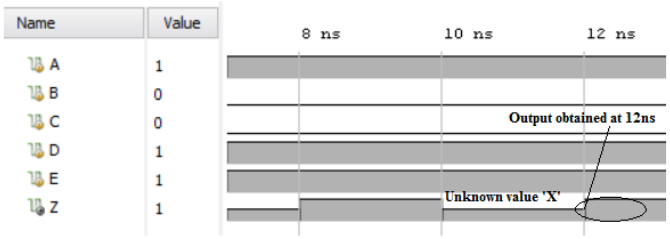

Fig. 8. Output with fault

During test mode of operation digital circuits are applied with huge number of test patterns. These test patterns suffer from excessive transition, which fakes the design to be a faulty one. Hence, it is necessary for a DFT engineer to differentiate between faulty and good chip.

The rest of the paper is organized as follows. Comparison of LOC and LOS scheme is presented in Section II. Survey on existing power minimization method is briefed in Section III. Section IV describes the tools required to implement the power minimization methods. Finally, Section V concludes the paper.

II. LOC AND LOS – A COMPARISON

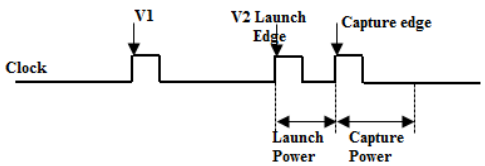

Fig. 9. Waveform – Launch and Capture power

Launch and capture power are two kinds of power occurs due to LOS and LOC schemes. Launch power is the measure of power from launch edge to capture edge when a transition is launched. Capture power is the measure of power from the capture edge. From literature [9] it is clear that launch power of LOS is 1.96 times higher than that of LOC launch and capture power.Fig. 9. shows the concept of launch and capture power in one clock cycle. At launch edge the transition is launched and it is captured at the capture edge.

In literature [9], it is found out that launch power of LOS is much higher than LOC in the presence of clock gates when compared with the absence of clock gates. This is because, half of the clocks are not active during launch cycle of LOC. Launch power of LOS is reduced by 11% with adjacent filling (or 0-filling) when compared with random filling. By making clock gates of LOS similar to LOC, the launch power can be further reduced. 20% reduction in peak switching activity with 80% increase in test volume is obtained by grouping flip flops with independent test enable control.

LOC is most often chosen over LOS because scan-enable control signal in LOS is hard to implement in most of the scan-based design. Also, LOS causes over testing which is also a case in LOC when more clock cycles are used. [10] presents the comparison of LOS and LOC schemes in terms of fault coverage and power consumption. It is clear that LOS achieves highest fault coverage than LOC,whereas LOC is better than LOS in terms of power consumption. Launch power of LOS canbe minimized by adjacent filling with the cost of fault coverage reduction and increased test length.

Comparison of LOC and LOS scheme in terms of fault coverage and test power of a multiple clock domain is presented in [11]. Test power minimization can be achieved by LOC scheme and fault coverage can be improved by LOS scheme. From literature it is proved that 30-50% power reduction can be achieved by LOC over conventional ATPG. 15-20% improvement in terms of fault coverage can be achieved by LOS. The preferred techniques to test the multiple clock domains are i) single capture, ii) skewed load and iii) double capture. 28.98% of power minimization is achieved by LOC and 21.6% by LOS. It is also suggested that fault coverage can be further improved by combining LOC and LOS.

Future work can be enhanced by combining LOS and LOC scheme to achieve highest fault coverage.

III. POWER MINIMIZATION METHODS

Miniaturization of digital world increases the demand of low power digital devices. Low power devices can be designed by the efficient powerminimization techniques like A. Low power ATPG, B. X filling techniques, C. Test vector ordering, D. Scan path organization and E. Clock gating.

A. Low power ATPG

Power at shift and capture mode can be minimized by effective ATPG patterns with less switching activity. Test patterns with high number of don't care bits prompt to shift power reduction. Insertion of clock gating cell reduces the number of flip flop which leads to the reduction of capture power [12]. 50% and 20% improvement in capture and shift power is achieved by the proposed method over ATPG with MT-fill.

Addition of rescue and mask phase during at-speed scan testing by modifying the ATPG generated test patterns, reduces Launch Switching activity (LSA)[13]. Three main idea behind reduction of LSA are i) risky path identification – process of identifying path with largest LSA ii) risky path reduction – reduction of LSA iii) risky path masking – placing X bit at the test response vector.

Capture power reduction is achieved by minimal launch weighted switching activity (WSA) obtained by introducing clock-gating and FF-activation reluctant (FAR-TPG) into test pattern generation stage. FAR-TPG achieves a good amount of fault coverage with limited activation of flip flops (FF). FF deactivation assigns logic '0' to clock signals and JP filling at FF silencing stage leads to minimal FF transition. 36.1% improvement in terms of launch WSA is achieved through the methodology proposed in [14].

Power during transition fault analysis is achieved by reduced switching activity through Bit Swapping-LFSR (BS-LFSR) and LOC scheme [15]. The architecture of pattern generator is modified by including a multiplexer unit with the LFSR to minimize the transition by swapping the neighboring bits. Transition deficiency is met by LOC scheme and power minimization is achieved by the usage of repeated patterns.

Two-time frame circuit model is proposed to generate test patterns without modifying the ATPG, for the stuck-at and transition fault which is transformed into a unified fault model [16]. 15% reduction of test pattern and test application time is observed when implemented with the ISCAS'89 and ITC'99 benchmark circuits.

B. X filling techniques

Reduction of power during transition fault testing can be achieved by lessen switching activity through efficient don't care filling. Power at launch-to-capture cycle in LOS scheme is minimized by test relaxation and X filling technique, in order, to lower the stress of the circuit. 0-fill, 1-fill and adjacent filling technique are chosen to minimize power consumption [17]. The circuit consumes more power due to the following reasons:

- Transition in the clock-tree and scan-enable tree

- Transition in scan cell
- Transition in combinational logic

Table Ibriefs the concept of X-filling by various methods. X bits in the test cube are filled by logic '0' in 0-fill. 1-fill fills the don't care bit with logic '1'. X bits are filled with the adjacent bits in adjacent fill.

Table- I: X-Filling Methods for the Test Cube

1XXXX0 0XXX10

Method	Resultant test cube
0-fill	1**0000**0 0**000**10
1-fill	1**1111**0 0**111**10
Adjacent-fill	1**1111**0 0**000**10

Transition in clock tree and scan enable tree are not considered in [17], because they are independent of test vector. Hence, X-filling is opted to minimize the transition in scan cell and combinational block. It is concluded that, functional power while considered as the target value, prevents test escapes due to excessive test power reduction.

Dynamic programming based X-filling [18] minimizes capture power of LOS testing through interval coloring problem by minimizing the input toggle of the circuit. Minimization of input toggle can be achieved by increasing the size of don't care stretches through Interleaved test vector ordering followed by the X-filling algorithm. Don't care bits are filled by either 0 or 1 logic in such a way that the hamming distance between the bits are minimized. 34% power saving is achieved when compared with 0-fill, 1-fill or adjacent-fill.

Minimization of capture power can be achieved by conducting X-filling on selected order of flip flop [19]. It can be met by increasing the number of flip flops without increasing the transition and also by selecting the flip flopbased on correlationthat do not transfer values. Condition to fill the don't care bits in the selected flip flop is toassign values with minimum transition. Correlation based X-filling is better than JP-fill by 6.5% improvement in weighted switching activity (WSA).

60% reduction of WSA is achieved through filling X-bits based on Integer Linear Programing (ILP) by which capture power minimization is achieved [20]. Filling of X-bits to minimize unnecessary switching activity is achieved by converting Boolean equation into linear equation and solving it.

C. Test vector ordering

Capture power can be minimized by ordering test vectors using artificial intelligence A^* search algorithm [21]. To choose a path with minimum number of transition, sum of the cost and heuristic function of the path is necessary. Capture power is minimized by choosing a path with minimal hamming distance between scan-out and scan-in vector.

Test vectors with don't care bits are ordered in such a way, that the combinational state between the capture cycles are preserved, would lead to the average reduction of launch-to-capture switching activity by 17.68% [22]. 43.5% reduction of capture power is achieved by the test vector ordering aware X-filling over the adjacent filling. The preferred X-filling methods are Random-fill and Adjacent pattern fill.

D. Scan path organization

Capture power during at-speed delay testing can be minimized by modifying the scan path. The scan path organization includes 3.4.1 scan chain partitioning 3.4.2 scan cell gating.

a. Scan chain partitioning

Partitioning the flip flops in the scan chain aslocal FF, incoming FF, outgoing FF and non-scan FF based on signal dependencies minimize the capture power during at-speed scan testing [23]. Activation of FF in the targeted partition reduces the capture power. Non-partitioned scan chain contributes to the 50% reduced WSA.

Scan flip flops are partitioned by partial launch-on-capture scheme and the overlapping part is kept smaller [24]. Some of the flip flops are only active during capture and launch cycles, therefore none of the testable broadside test remains untested and so the capture power is reduced compared to preferred fill.

Fault coverage of multiple capture cycle is maintained on grouping scan cells based on Integer Linear Programming (ILP) [25]. This, can be achieved by minimizing the data dependency between the scan flip flop. Peak and average capture power reduction is achieved by 45.53% and 48.9% in comparison with the existing scan chain partitioning methods.

Minimization of capture power in logic BIST is achieved by partitioning the scan chain based on signal probability analysis [26]. Peak and average capture power reduction of 39% and 50% respectively, is achieved

by adding more number of don't care bits to the test pattern and by activating limited number of flip flops during scan cycles.

b. Scan cell gating

The concept of scan cell gating is shown in Fig. 10. The gating logic is preferred to minimize the capture power during scan testing.

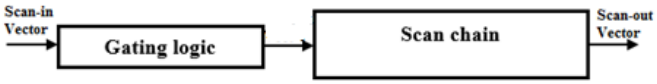

Fig. 10. Scan cell gating

Block enable cells inserted into the scan chain blocks the transition at scan cells from propagating into the combinational block, thus capture power is minimized [27]. Control information to block transition at capture phase in a scan chain is transmitted along with scan-in data, thereby eliminating the usage of additional control pins.During first capture cycle with 50% threshold, 31.74% and 26.51% of average and peak capture power reduction are achieved. At second capture cycle 35.44% and 34.70% reduction of peak and average capture power are obtained.

Decoder and AND gate acts as a gating logic to disable the scan cells during capture cycle[28]. 39.81% of capture power reduction is observed, when implemented with ISCAS'89 benchmark circuits.Power at shift and capture mode is balanced by complementary pair of weight. The output of selected power sensitive cells is freezedby partial gating logic [29] based on toggling probability. 6% improvement in capture power increment rate is observed.

Scan output are gated by pull-up and pull-down transistor with sleepy stack inverter [30]. Switching activity in scan chain is shortened by adding inverted scan cell into the scan chain. 22.53% power improvement is observed over other modified scan cells.

E. Clock gating

The concept of clock gating is shown in Fig. 11. The clock to the flip flop is gated by the gate cell to reduce the power consumption during scan testing.

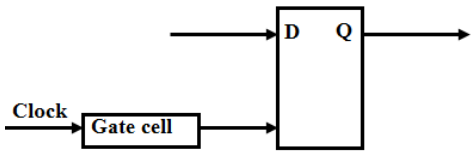

Fig. 11. Clock gating

Selective holding of certain scan flip flops by clock gating leads to 55% reduction of average capture switching [31]. On filling don't care bits with scan unload values, capture switching activity is reduced. Also, on filling with other values leads to the increase in transition.Capture transition get reduced by gating the clock to the flip flop, only in the presence of more care bits.

Partitioning the clock gates and grouping of flip flops minimizes the capture power during scan testing without modifying the test patterns and with minimum hardware overhead and maximum fault coverage [32]. AND gate acts as a clock gate followed by a transition controller, scan flip flop and decoder unit. Capture power budget is maintained at about 25%.

Transition on clock tree leads to excessive switching, so, the clock tree is disabled by a control logic comprising XOR gates, register and a biasing logic leads to low power consumption [33]. The concept of clock gating is implemented in 5 industrial circuits and an average reduction of capture switching activity by 22.52% is noted.

Capture power minimization by clock gating is carried out on a 45nm SoC [34]. OR gate, AND gate and a latch are the preferred clock gating logic. Test hooks acts as a test enable control to clock gate. Power grid addresses the problem of IR drop and vertex coloring automatically gates the clock signal. An average of 42.82% power improvement is noted at the industrial SoC's.

IV. IMPLEMENTATION TOOLS

Techniques like low power ATPG, X filling techniques, test vector ordering, scan path organization and clock gating which are meant to minimize capture power can be implemented and verified using ISCAS benchmark circuits. Combinational circuits are grouped under ISCAS'85 and sequential circuits under ISCAS'89 benchmark circuits [35,36]. These circuits are primarily meant for testing.

Table 2: List of Software

TOOLS	MODE OF OPERATION
Tetra MAX	Test pattern generation
Mentor Graphics	
MINTEST	
HOPE	
ATLANTA	
SYNOPSYS Design Compiler	Synthesize
CADENCE	
XILINX	
TSPICE	Simulation
MODELSIM	

Table 2.lists the tools preferred during testing. Major test pattern generator vendors are SYNOPSYS and Mentor graphics. ATLANTA tool is specially meant for generating test patterns for combinational circuits and HOPE for synchronous sequential circuits by FAN algorithm and parallel fault simulation [37, 38, 39]. Power utilization can be effectively calculated by SYNOPSYS design compiler and XILINX. Simulation of power minimization method can be done by MODELSIM and TSPICE.

V. CONCLUSION

Based on survey, itis concluded that fault coverage can be met by LOS scheme and reduction of power by LOC scheme. On combining X-filling techniques with test vector ordering, scan path organization and clock gating, a remarkable amount of power minimization can be achieved. Combination of LOS and LOC schemes is proposed for the future work to achieve highest fault coverage and develop an efficient power minimization technique.

REFERENCES

[1] Clary and Sacane, "Self-Testing Computers," in *Computer*, vol. 12, no. 10, pp. 49-59, Oct. 1979.

[2] E. J. McCluskey, "Built-In Self-Test Techniques," in *IEEE Design & Test of Computers*, vol. 2, no. 2, pp. 21-28, April 1985.

[3] S. Chakravarty and V. P. Dabholkar, "Two techniques for minimizing power dissipation in scan circuits during test application," *Proceedings of IEEE 3rd Asian Test Symposium (ATS)*, Nara, Japan, 1994, pp. 324-329.

[4] M. Geilert, J. Alt and M. Zimmermann, "On the efficiency of the transition fault model for delay faults," *1990 IEEE International Conference on Computer-Aided Design. Digest of Technical Papers*, Santa Clara, CA, USA, 1990, pp. 272-275.

[5] M. Tehranipoor and K. M. Butler, "Power Supply Noise: A Survey on Effects and Research," in *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 51-67, March-April 2010.

[6] J. A. Waicukauski, E. Lindbloom, B. K. Rosen and V. S. Iyengar, "Transition Fault Simulation," in *IEEE Design & Test of Computers*, vol. 4, no. 2, pp. 32-38, April 1987.

[7] J. Kõusaar and R. Ubar, "7-valued algebra for transition delay fault analysis," *2014 14th Biennial Baltic Electronic Conference (BEC)*, Tallinn, 2014, pp. 89-92.

[8] J. Savir and S. Patil, "Scan-based transition test," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 8, pp. 1232-1241, Aug. 1993.

[9] J. Savir and S. Patil, "Broad-side delay test," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 8, pp. 1057-1064, Aug. 1994.

[10] K. Agarwal, S. Vooka, S. Ravi, R. Parekhji and A. S. Gill, "Power Analysis and Reduction Techniques for Transition Fault Testing," *2008 17th Asian Test Symposium*, Sapporo, 2008, pp. 403-408.

[11] F. Wu *et al*., "Analysis of power consumption and transition fault coverage for LOS and LOC testing schemes," *13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems*, Vienna, 2010, pp. 376-381.

[12] S. Pandey, N. S. Murty and R. Ranjan, "Test Power and Transition Fault Coverage Comparison Between LOC and LOS Test Scheme for Multiple Clock Domain Circuits," *2017 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC)*, Coimbatore, 2017, pp. 1-4.
[13] S. Khullar and S. Bahl, "Power Aware Shift and Capture ATPG Methodology for Low Power Designs," *2011 Asian Test Symposium*, New Delhi, 2011, pp. 500-505.
[14] X. Wen *et al*., "Power-aware test generation with guaranteed launch safety for at-speed scan testing," *29th VLSI Test Symposium*, Dana Point, CA, 2011, pp. 166-171.
[15] Y. Lin, J. Huang and X. Wen, "Clock-gating-aware low launch WSA test pattern generation for at-speed scan testing," *2011 IEEE International Test Conference*, Anaheim, CA, 2011, pp. 1-7.
[16] M. Vignesh and J. Jayaseelan, "Transition faults test pattern generation for minimizing power using BS-LFSR and LOC," *2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]*, Nagercoil, 2015, pp. 1-6.
[17] Y. Kung, K. Lee and S. M. Reddy, "Generating Compact Test Patterns for Stuck-at Faults and Transition Faults in One ATPG Run," *2018 IEEE International Test Conference in Asia (ITC-Asia)*, Harbin, 2018, pp. 1-6.
[18] F. Wu *et al*., "Power reduction through X-filling of transition fault test vectors for LOS testing," *2011 6th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Athens, 2011, pp. 1-6.
[19] "DP-fill: A dynamic programming approach to X-filling for minimizing peak test power in scan tests," *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, 2015, pp. 836-841.
[20] M. Yoshimura, Y. Takahashi, H. Yamazaki and T. Hosokawa, "A Don't Care Filling Method to Reduce Capture Power Based on Correlation of FF Transitions," *2015 IEEE 24th Asian Test Symposium (ATS)*, Mumbai, 2015, pp. 13-18.
[21] R. Gulve and V. Singh, "ILP based don't care bits filling technique for reducing capture power," *2016 IEEE East-West Design & Test Symposium (EWDTS)*, Yerevan, 2016, pp. 1-4.
[22] U. S. Mehta, K. S. Dasgupta, N. M. Devashrayee and H. Parmar, "Artificial intelligence based scan vector reordering for capture power minimization," *2011 Nirma University International Conference on Engineering*, Ahmedabad, Gujarat, 2011, pp. 1-6.
[23] Potluri, Seetal&SatyaTrinadh, A &BabuCh, Sobhan&Kamakoti, V and Chandrachoodan, Nitin, "DFT Assisted Techniques for Peak Launch-to-Capture Power Reduction during Launch-On-Shift At-Speed Testing," *ACM Transactions on Design Automation of Electronic Systems.* Vol. 21, No. 1, pp. 1-25, 2015.
[24] H. F. Ko and N. Nicolici, "Automated Scan Chain Division for Reducing Shift and Capture Power During Broadside At-Speed Test," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 11, pp. 2092-2097, Nov. 2008.
[25] Z. Chen and D. Xiang, "Low-capture-power at-speed testing using partial launch-on-capture test scheme," *2010 28th VLSI Test Symposium (VTS)*, Santa Cruz, CA, 2010, pp. 141-146.
[26] Z. Chen, K. Chakrabarty and D. Xiang, "MVP: Capture-power reduction with minimum-violations partitioning for delay testing," *2010 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, 2010, pp. 149-154.
[27] N. Li, E. Dubrova and G. Carlsson, "A scan partitioning algorithm for reducing capture power of delay-fault LBIST," *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, 2015, pp. 842-847.
[28] X. Lin and J. Rajski, "Test Power Reduction by Blocking Scan Cell Outputs," *2008 17th Asian Test Symposium*, Sapporo, 2008, pp. 329-336.
[29] Jiann-Chyi Rau, Po-Han Wu and Ming-Ying Chiang, "A novel gated scan-cell scheme for low Capture Power (LCP) in at-speed testing," *Proceedings of the 2009 12th International Symposium on Integrated Circuits*, Singapore, 2009, pp. 647-650.
[30] W. Zhao, M. Tehranipoor and S. Chakravarty, "Power-safe test application using an effective gating approach considering current limits," *29th VLSI Test Symposium*, Dana Point, CA, 2011, pp. 160-165.
[31] S. Ukey, S. Rathkanthiwar and S. Kakde, "VLSI implementation of low power scan based testing," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0866-0870.
[32] K. Chakravadhanula, V. Chickermane, B. Keller, P. Gallagher and P. Narang, "Capture power reduction using clock gating aware test generation," *2009 International Test Conference*, Austin, TX, 2009, pp. 1-9.
[33] B. Yang, A. Sanghani, S. Sarangi and C. Liu, "A clock-gating based capture power droop reduction methodology for at-speed scan testing," *2011 Design, Automation & Test in Europe*, Grenoble, 2011, pp. 1-7.

[34] J. Rajski, E. K. Moghaddam and S. M. Reddy, 0"Low power compression utilizing clock-gating," *2011 IEEE International Test Conference*, Anaheim, CA, 2011, pp. 1-8.
[35] R. Shaikh *et al.*, "At-speed capture power reduction using layout-aware granular clock gate enable controls," *2014 International Test Conference*, Seattle, WA, 2014, pp. 1-10.
[36] F. Brglez, H. Fujiwara, "A Neutral Netlist of 10 Combinational Benchmark Circuits and a Target Translator in Fortan," *in Proc. of the International Symposium on Circuits and Systems*, pp. 663-698,1985.
[37] F. Brglez, D. Bryan, K. Kozminski, "Combinational Profiles of Sequential Benchmark Circuits," *in Proc. of the International Symposium of Circuits and Systems*, pp. 1929-1934, 1989.
[38] H.K. Lee and D.S. Ha, "Atalanta: an Efficient ATPG for Combinational Circuits,"*Technical Report, 93-12, Dep't of Electrical Eng.*, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, 1993.
[39] H.K. Lee and D.S. Ha, "An efficient forward fault simulation algorithm based on the parallel pattern single fault propagation," *Proc. Int. Test Conf.*, pp. 946-955, October 1991.
[40] H. K. Lee and D. S. Ha, "HOPE: An Efficient Parallel Fault Simulator for Synchronous Sequential Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, pp. 1048-1058, September 1996.

Asha pon. S, received the B.E degree in Electronics and communication engineering, in 2013 and M.E degree in VLSI, in 2015 from Anna University, Tamilnadu, India. She is currently pursuing Ph.D. degree in Information and communication from the Department of Electronics and Communication engineering, College of Engineering, Guindy, Anna University, Tamilnadu, India.
Her current research interests include low power scan testing and delay testing.
Jeyalakshmi. V (Member ISTE,IETE) received the B.E and M.E degrees from the Madurai kamaraj University and Ph.D degree in information and Communication from Anna University, Tamilnadu, India.

Dr. Jeyalakshmi. V, working as a Professor in Electronics and Communication Engineering at College of Engineering, Guindy, Anna University, Chennai, Tamilnadu, India. She has more than 20 years of teaching experience. She has published more than 29 papers in journals and 22 papers in conferences. She was a principal investigator involved in MOOC, and funded by MHRD at EMMRC during 2016. Her research interests are Digitization, IOT, VLSI, Signal Processing, Mobile Communication, Networking and MEMS.

S. Asha Pon. "Review of Power Minimization Techniques in Transition Fault Testing." *IOSR Journal of Engineering (IOSRJEN)*, 10(2), 2020, pp. 0715.