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A Novel FPGA Based Synchronous High Resolution Digital Pulse Width Modulators for Inverters

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Abstract: - This paper presents the survey of Pulse Width Modulators for inverters. Pulse Width Modulators are widely used as the basic block for controlling the on and off of the load that connecting with the inverter. Here presents two synchronous techniques that increase the resolution of Pulse Width Modulation. The synchronous techniques based on on-chip DCM (Digital Clock Manager) present in Spartan 3 FPGA series and the second technique based on IODELAYE1 block present in the Virtex 6 FPGA series. The two techniques fully avoid glitches and improve the reliability of the circuit. The circuit also uses the coarse resolution counter and one or two DCM or IODELAYE1 blocks. The PWM is set in the beginning of the counter and resets based on certain fraction of clock periods. The first architecture, presents the generalization of DCM based circuit and it allows operating the circuit at higher clock frequencies. The second is based on the I/O delay element (IODELAYE1) available in the Virtex-6 FPGAs, and it provides higher resolution with a straightforward implementation

Keywords: - *Field programmable gate arrays (FPGA), power conversion, Digital clock manager, IODELAYE1, Pulse Width Modulators.*

I INTRODUCTION

Digital pulse width modulators (DPWMs) have become an integral part of almost all embedded systems. It has been widely accepted as control technique in electronic appliances. One of the applications of DPWM lies in power electronics for controlling power converters (DC/DC, DC/AC, etc.). PWM inverters are one of those power converters which extensively use concept of PWM for its operation. PWM circuits output a square waveform with a varying on to off ratio. The average ratio can vary from 0 to 100 percentage. This on time (TON) to off time period (T) ratio is called as duty cycle, which is expressed in percentage. There are basically two PWM techniques, Analog PWM generation technique and Digital PWM generation technique. Digital controls are increasingly used in power converters because of their advantage when compared to analog controls. The main advantages of using digital controls over analog are the ability to perform more advanced and sophisticated functions that potentially result in improving power conversion efficiency and/or dynamic performance of the power converter, the ease of digital control function and loop upgradeability, and reduced sensitivity to component variations compared to analog controllers. Digital pulse width modulators mainly work as basic building block in digital control architectures of any power converters. The simple PWM diagram is shown in figure.1.

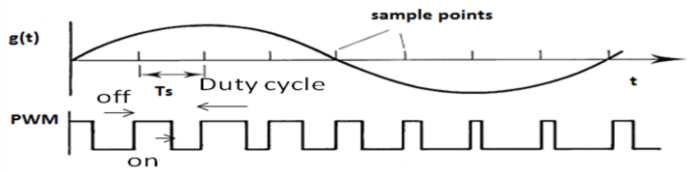

Figure1.Simple PWM

II SYSTEM ARCHITECTURE

In the PWM design, the resolution and synchronization determines the accuracy in the output voltage/current control of any power converters. The architectures explained here based on two fully synchronous designs using different FPGA resource the DCM and the I/O delay element (IODELAYE1).The DCM-based architecture uses the Digital Clock Manager block present in the Spartan-3 FPGA and the I/ODELAYE1-based architecture uses the I/O delay element block available in Virtex- 6 FPGA series. These

architectures mainly used to achieve higher resolution PWMs. Besides, these are glitch free designs, which improve the circuit reliability and the number of paths to equilibrate in order to achieve a monotonic behavior is minimized.

III DCM BASED HRPWM ARCHITECTURE

The first architecture explains the input clock is given to the Digital Clock Manager block present in the Spartan-3 FPGA. The DCM generates the frequency synthesized output for resolution and the quadrant phase shifted output for synchronization. The frequency synthesized output goes to the counter and quadrant phase shifted output to the multiphase circuit. The PWM set at the beginning of the counter and reset after a given number of clock cycles plus a certain fraction of the clock period established by the DCM. The digital circuit used for delaying the reset signal is fully synchronous. The set and reset of the SR flip-flop determines the PWM output.

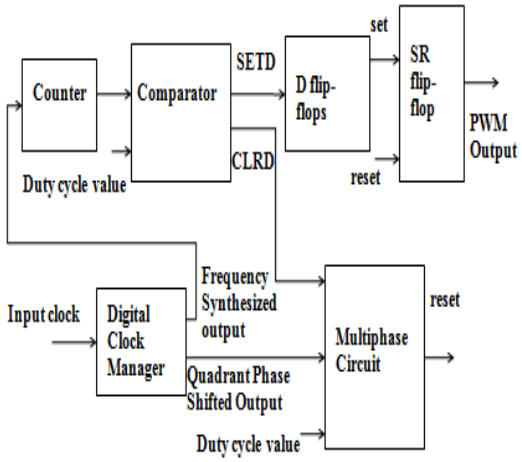

Figure.2. DCM Based Implementation of PWM

A.Digital Clock Manager

DCM is the clock management block present in the Spartan-3 FPGA series. It provides advanced clocking capabilities to Spartan-3 FPGA applications.

DCM solves the common clocking issues by

- shifting the clock
- condition the clock
- multiplying the incoming clock signal
- eliminating the clock skew

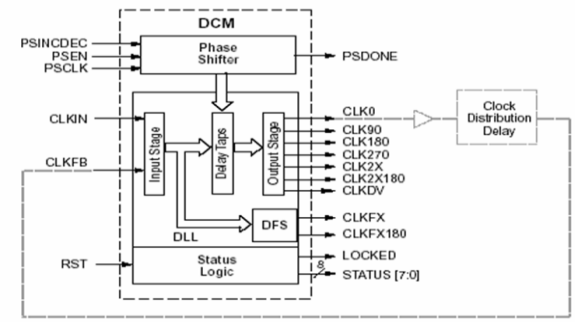

Figure 3. Functional Block of DCM

DCM mainly consist of four functional blocks namely

- Phase Shifter
- Digital Frequency Synthesizer
- Delay Locked Loop

- Status Logic

(1)Delay-Locked Loop (DLL)

The Delay-Locked Loop (DLL) unit provides an on-chip digital deskew circuit that generates zero-propagation-delay clock output signal. The input signals to the DLL unit are CLKIN and CLKFB. The output signals from the DLL are CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV. The DLL unit generates the outputs for the Clock Doubler (CLK2X, CLK2X180), the Clock Divider (CLKDV) and the quadrant phase shifted output functions.

(2)Digital Frequency Synthesizer

The Digital Frequency Synthesizer (DFS) provides a wide and flexible range of output Frequencies based on the ratio of two user-defined integers, a multiplier (CLKFX_MULTIPLY) and a divisor (CLKFX_DIVIDE). The output frequency is derived from the input clock (CLKIN) by simultaneous frequency division and multiplication. The DFS unit generates the Frequency Synthesizer (CLKFX, CLKFX180) output

(3)Phase Shifter

The Phase Shift (PS) unit controls the phase relations of the DCM's clock outputs to the CLKIN input. The phase shift unit also provides a digital interface for the FPGA application to dynamically advance or retard the current shift value by 1/256th of the clock period.The input signals to the Phase Shift unit are PSINCDEC, PSEN, and PSCLK. The output signals are PSDONE and the STATUS [0] signal.

(4)*Status logic*

The status logic indicates the current state of the DCM via the LOCKED and STATUS [0] STATUS [1] and STATUS [2] output signals. The LOCKED output signal indicates whether the DCM outputs are in phase with the CLKIN input. The STATUS output signals indicate the state of the DLL and PS operations.

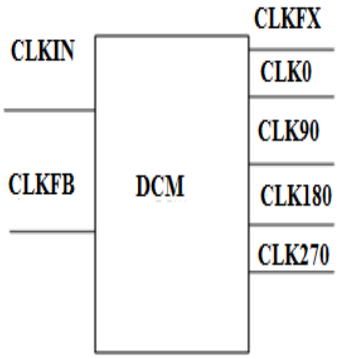

Figure 4.Simplified Pin Out Of DCM

The RST input signal resets the DCM logic and returns it to its post-configuration state. Likewise, a reset forces the DCM to reacquire and lock to the CLKIN input. The key of this architecture is the on-chip DCM block provided in almost every state of the art FPGA. The DCM provides four quadrant phase-shifted clock signals derived from the source clock CLKIN. In addition to CLK0 for zero-phase alignment to the CLKIN signal, the DCM also provides the CLK90, CLK180 and CLK270 outputs for 90,180and 270 phase-shifted signals, respectively. Besides, all the outputs of the DCM can be phase shifted with finer resolution.

The DCM can generate a wide range of output clock frequencies (CLKFX output port), performing clock frequency division and multiplication. Besides this phase shifting, the DCM is able to obtain clock outputs with 50% duty cycle. The clock feedback signal CLKFB is used to compare and lock the output signals with the input CLKIN signal. The fine phase shifting can be fixed or variable. It is set by means of the DCM attribute PHASE_SHIFT, an integer in the range [−255, +255].

B. Multiphase Circuit

The multiphase circuit consists of D-flip-flops and the multiplexer. The number of flip-flop required according to the number of DCM present in the design. If the design consist of 'r' DCMs then the number of

flip-flops used as p=4*r. The multiplexer output is any one of the flip-flop output. So the multiplexer used here is generalized as p to 1 multiplexer.

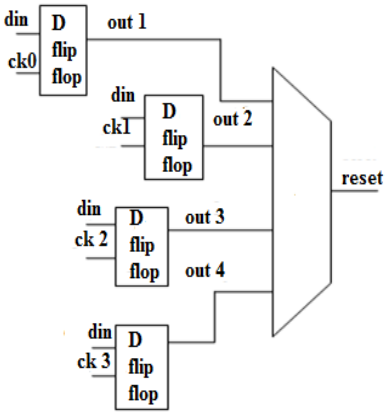

Figure 5. Multiphase Circuit

The D flip-flop is used to delay the reset signals. The clocks coming from the quadrant phase shifted output of DCM is used as the clock of the different flip-flops. The 'din' value of all the flip-flop is same and the output depends on the positive edge of the clocks from the quadrant phase shifted clocks. The multiplexer is used to select any one of the flip flops output by using the least significant bits of the duty cycle value as the select bit.

IV IODELAYE1 BASED HRDPWM

In the IODELAYE1 BASED HRPWM the input clock is given to the MMCM and the frequency synthesized outputs of the MMCM are given to the counter and the I/O delay element. The counter is used to count the values and the comparator is used to generate the SET and CLRD signals used to control the SR flip-flop. The I/O delay element is used to generate the delay in the reset signal .The digital circuit used for this purpose is a fully synchronous one. The set and reset of the SR flip-flop gives the PWM output. Here the MMCM that produces the multiple clock frequencies used for synchronization purpose.

A.Mixed Mode Clock Manager

MMCM is the clock management resource present in the clock management tile of Virtex6 FPGA. The MMCM primitive in Virtex-6 parts is used to generate multiple clocks with defined phase and frequency relationships to a given input clock. The functional diagram shown in figure.5.The MMCM module takes an input clock named CLKIN1 and generates several output clocks, each of which can be configured to have a different frequency that is dependent on the input clock frequency. The MMCM module encapsulates the MMCM_ADV primitive. It produces 8 independently programmable outputs.

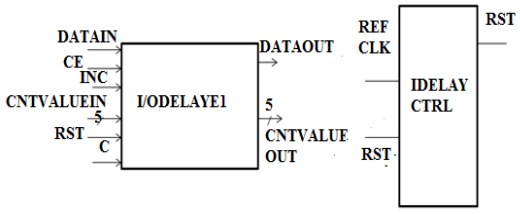

Figure 6. Simplified Pin Out Of (a) IODELAYE1 (b) IDELAYCTRL.

(1) O0 to O6 and CLKFBOUT.

(2) O0 to O3 offers true complementary output.

Phase / frequency detector compares CLKIN with CLKFB and it accepts up to 650-MHz inputs and adjusts the charge pump output voltage higher or lower. Charge pump is used to control the VCO frequency. Many different output frequencies can be generated by using the equation:

Fout = Fin * M / (D*O).

Each MMCM consists of only one M and D value and each MMCM output can have its own O value. The values of M, D and R ranges are M: 1…64; D: 1…80; O: 1…128. Locked signal shows the MMCM locked on the input frequency. CLKINSTOPPED/FBSTOPPED is the status signals indicating that the input or feedback clocks have stopped running. The frequency synthesised output is obtained here by using the by using M=8, D=2, O1=2, O2=4 .The two frequency syn

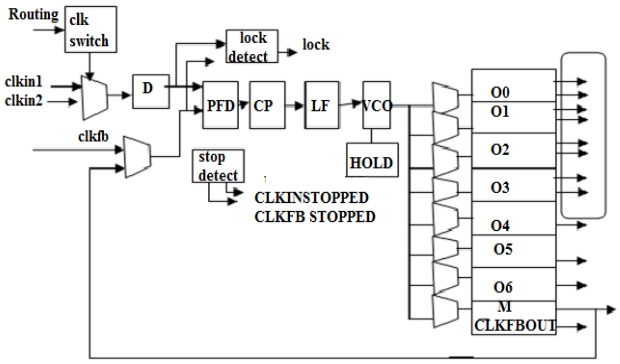

Figure 7.MMCM internal

B.I/ODELAYE1

Virtex6 I/O block contains a programmable absolute delay element called IODELAYE1. IODELAYE1 is a 31-tap, wraparound, delay element with a calibrated tap resolution. IODELAYE1 allows incoming signals to be delayed on an individual basis. The tap delay resolution is varied by selecting an IDELAYCTRL reference clock from the range specified in the Virtex-6 FPGA data sheet. The IODELAYE1 resource can function as IDELAY, ODELAY, or bidirectional delay The MMCM output given as the clock of the IODELAY.T he IODELAYE1 block offers three different operational modes when operating in the unidirectional input delay configuration, depending on the mechanism used to select the number of delay taps. The RST, CE, INC are the signals to control the tap delay.

1) ***Fixed*****:** The number of delay taps is predefined through the block attributes and it cannot be changed during operation.

2) ***Variable*****:** The number of delay taps can be dynamically changed after configuration through the control signals CE and INC. When the enable increment/decrement signal (CE) is activated, the number of delay taps increases or decreases depending on whether the INC signal is activated or not. If the reset signal RST is activated, the delay value is reset to a predefined value .The simplified pin out of IODELAYE1 and IDELAYCTRL.

3) ***Loadable Variable*****:** This mode has the same functionality as the *variable mode*. In addition to this, it allows loading the delay value through the 5-bit input. CNTVALUEIN When in this mode, the IODELAYE1 reset signal resets the delay value to a value set by the CNTVALUEIN.

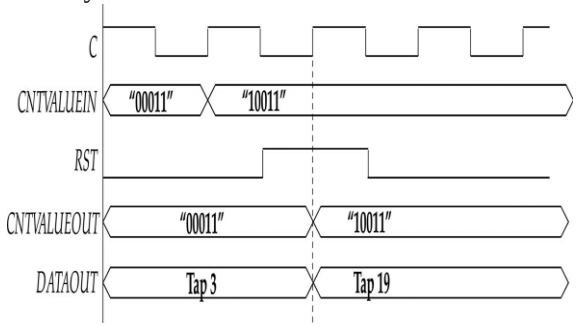

Figure 8. IODELAYE1 Operation in Loadable Variable Mode. *Architecture*

Figure6. shows the proposed implementation for an m+1-bit HRPWM. Basically, the proposed circuit is made up of a synchronous m−4 bit counter, an IODELAYE1 block, two edge triggered flip-flops, an MMCM, and an SR latch whose output is the PWM signal. The main difference with the DCM based architecture is that the multiphase synchronous circuit used to generate the signal RESET is replaced by the IODELAYE1 block, making the implementation easier.

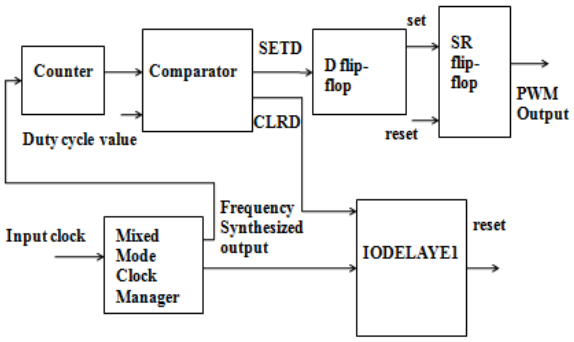

Figure 9..IODELAYE1 BASED HRPWM

Signals SETD and CLRD are generated as previously explained by comparing the counter output CNT with the most m−5 significant bits of the duty command dc(m:5). FFa and FFb are placed in order to avoid the glitches that may be present in the output of the comparator. For this implementation, the *loadable variable mode* for the IODELAYE1 block is used. The IODELAYE1 block allows, therefore, delaying the input signal through a 5-bit value CNTVALUEIN updated when the NVALUE signal is activated, which has to be synchronized with the clock C.

Considering that the maximum 32-tap delay covers half a period of CK_REF, a clock that doubles the CK_REF frequency is required to clock the counter. These clock signals are generated through the MMCM using as a reference the board base clock CK. The output frequency for the MMCM output *i* is set through its attributes *M*, *D*, and *Oi* as *f*CK*Oi* = *M*/(*D***Oi*). In addition to this, the IDELAYCTRL is instantiated in order to autocalibrate the delay tap as previously explained. Fig.9 shows the basic operation of the proposed IODELAYE1-based HRPWM architecture with dc = "10010011" The CLRD signal is activated when dc(7:5) = CNT(7:5) = "100" = 4. The resulting pulse is captured in the next clock cycle by FFb, which generates the input signal for the IODELAYE1 block DATAIN. The IODELAYE1 block generates the RESET signal by delaying the CLR signal a number of tap cycles given by dc (4:0) = "10011" = 19. This signal clears the SR latch to generate the desired PWM signal

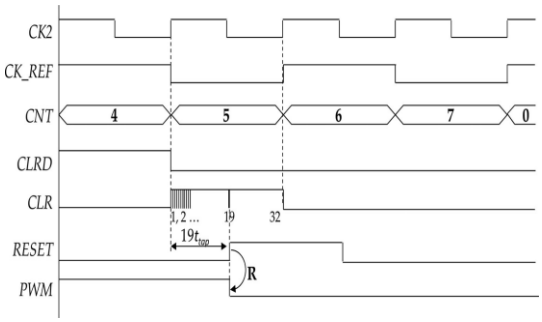

Figure.10. IODELAYE1-Based HRPWM operation with dc = "10010011."

V RESULTS AND DISCUSSIONS

This section presents the main experimental results for the two different PWM architectures. The DPWM signal frequency and duty cycle have been selected for test purposes. Fig.8 shows the experimental results for DCM based HRPWM architecture.

In this stage we give the input to the architecture, we set the clock input value in our implementation side the clkin act as clock input. If we give the input to the DCM block the output pulse and also the counter values are changed based upon the given input.

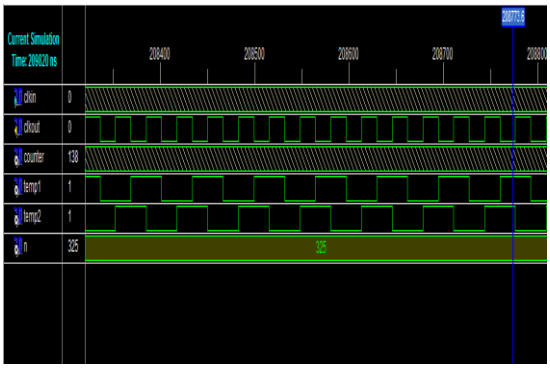

Figure.10. Simulation results of DCM based PWM

In this situation we achieve a synchronous in DCM block. In this stage we use the 50 percent duty cycle for the pulse generation which means half the time the pulses will be on and off. The counter value is changed. In first time we set the input value after that the pulses will be generated automatically. By this way we generate high resolution digital PWM signals. Here 'n' is the no:of bits.This allows an efficient HRPWM implementation for low cost systems.The experimental results for the IODELAYE-1 based HRPWM architecture are shown in fig.9.

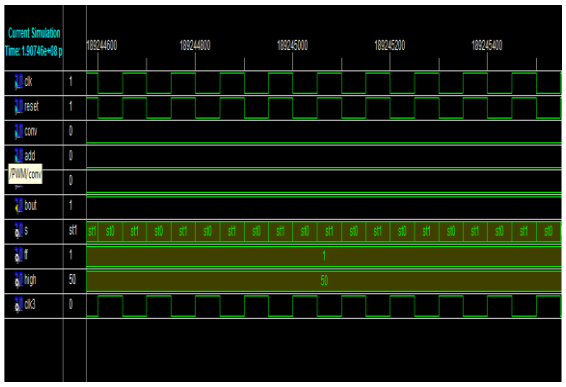

Figure.11.Simulation result of IODELAY based PWM

In contrast, the IODELAYE1-based architecture achieves a higher resolution by using the resources present in the high-endVirtex-6 FPGA series. This architecture features a straightforward implementation as it uses a single block instead of the multiphase circuit. The architecture is simplified and there is no need to equilibrate the propagation paths. One of the main advantages of this proposal compared to the previous one is that it allows generating as many PWMs as needed, as each I/O tile in Virtex-6 FPGAs contains two IODELAYE1 blocks. This architecture is therefore, recommended for systems requiring higher resolution or a high number of PWM outputs

.

VI CONCLUSION

The proposed DCM-based and IODELAYE1-based synchronous architectures have been designed on a Xilinx Spartan-3E and Virtex-6 FPGA, respectively. The experimental results show a resolution of 625ps for the DCM-based architecture, 78ps for the IODELAYE1-based architecture, and 19.5ps for the HRPWM architecture. The selection of the target device depends on the system cost and resolution requirements. The PWM developed can be used in many diverse and complex applications like robotics, motor and motion control.

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