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# An FPGA Based Implementation for 2-D Discrete Wavelet transform

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***ABSTRACT*:** A 2-D discrete wavelet transform hardware design based on multiplier design based architecture is presented in this paper. We have proposed based on arithmetic for low complexity and efficient implementation of 2-D discrete wavelet transform. The multiplier design based technique has been applied to reduce the number of delay. This paper provides the clearcut idea in about the application of 8-multiplier and 6-adder in one, two & three level of architecture This architecture is suitable for high speed on-line applications, the most important one being image processing, reduced the area and power in the discrete wavelet transform. With this architecture the speed of the 2-D discrete wavelet transform is increased. It has 100% hardware utilization efficiency

***KEYWORDS*:** *2-D Discrete wavelet transform (DWT), one level multiplier based design, two level multiplier based design, three level multiplier based design, multiplier based design scheme, Xilinx simulation***.**

## I. INTRODUCTION

Wavelets, based on the time-scaling representations provide an alternative to the time-frequency representation in signal processing domain. The shifting (or translation) and the scaling (or dilation) are unique to wavelets. The wavelet is a kind of bases which are generated by dilation and translation of a function [1], [2]. The wavelet analysis method has a good ability at localizing signal in both time and frequency plane[3].Due to the characteristic of flexible TF decomposition, DWT has also been widely used in many applications, especially in image and video coding, speech and audio coding, speech enhancement, speech recognition, hearing aid and digital commutation [2],[3],[4].

Silicon-area, speed, power consumption and design cost are the general parameters that are taken care while designing VLSI architecture, DSP system and high performance system. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. Earlier, power consumption was a secondary concern in comparison to area and speed. However, inrecent years, power is being given more importance as area and speed due to phenomenal growth of portable and wireless handheld multimedia devices. The power consumption is the most critical design concern for these devices [5].

Comparing the 2-D DWT with the 1-D DWT, we find that the difference is that in the 1-D DWT the range of operation is halved with a change in decomposition level j, while in the 2-D DWT the range of operation is always the whole frame. So as the operation range halved with the increase in decomposition level, the above structure can perform the 1-D DWT easily.

In this paper, we have introduced a new architecture for the 2-D discrete wavelet transform using multiplier design based (MDB)architecture. The algorithm for the tree structure of discrete wavelet transform is analyzed in the section II. Low-complexity designs for 2-D DWT in the section III.Propose architecture for multiplier design based in the section IV. Discuss the simulation result and conclusion in the section V&VI

## II. DISCRETE WAVELET TRANSFORM

The model used in [5] to implement the tree structure of Discrete Wavelet Transform (DWT) is based on the filtering process. Figure 1 depicted a complete 3-level discrete WPT. In this figure G and H is the high pass and low pass filter respectively.

Computation period is the number of the input cycles for one time produces output samples. In general, the computation period is M= for a j-level DWT. The period of the 3-level computation is 8. Figure 1, The Sub band Coding Algorithm As an example, suppose that the original signal X[n] has N- sample points, spanning a frequency band of zero to π rad/s. At the first decomposition level, the signal passed through the high pass and low pass filters, followed by subsampling by 2. The output of the high pass filter has N/2- sample points (hence half the time resolution) but it only spans the frequencies □/2 to □ rad/s (hence double the frequency resolution).

The output of the low-pass filer also has N/2- sample points, but it spans the other half of the frequency band, frequencies from 0 to □/2 rad/s. Again low and high-pass filter output passed through the same low pass and high pass filters for further decomposition. The output of the second low pass filter followed by sub sampling has N/4 samples spanning a frequency band of 0 to □/4 rad/s, and the output of the second high pass filter followed by sub sampling has N/4 sample

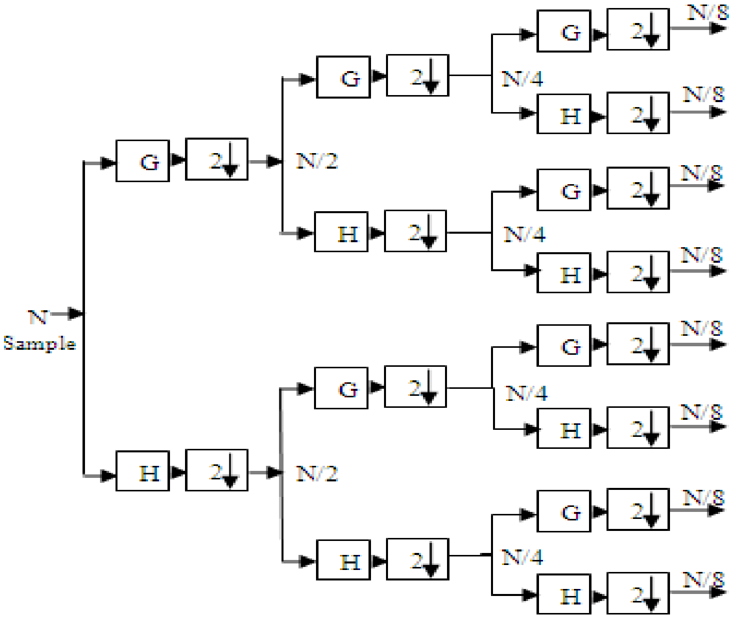


**Figure 1**: 3- Levels for DWT. Where G, H are High-pass and Low-pass Filter Coefficient.

spanning a frequency band of □/4 to □/2 rad/s. The second high pass filtered signal constitutes the second level of DWT coefficients. This signal has half the time resolution, but twice the frequency resolution of the first level signal. This process continues until two samples are left. For this specific example there would be 3 levels of decomposition, each having half the number of samples of the previous level.

The DWT of the original signal is then obtained by concatenating all coefficients starting from the last level of decomposition (remaining two samples, in this case). The DWT will then have the same number of coefficients as the original signal.

## III. LOW-COMPLEXITY DESIGNS FOR 2-D DWT

2-D DWT computation is nothing but two-channel FIR filter computation. Low-pass and high-pass down sampled filter computations are performed on the input to calculate the DWT coefficients. Low-pass down sampled filter is the average between two samples and high-pass filter is the difference b/w two samples. The DWT algorithms for 1-level decomposition are given as;

$$Y_{high}[k] = \sum_n h[n] * x[2k-n] (1)$$

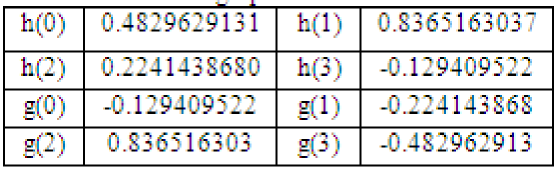
$$Y_{low}[k] = \sum_n g[n] * x[2k-n] (2)$$

Where x(n) is the input and $Y_{high}[k]$&$Y_{low}[k]$ are respectively

the low-pass and high-pass DWT coefficients, h[n] and g[n] are respectively, the low-pass and high-pass filter coefficients. We have assumed the Daubechies four tap (Daub-4) filter coefficients for the low-pass filter proposed design. However, similar type of design can be derived for other type of wavelet filters as well. The Daub-4 low-pass filter coefficients are taken from [7]. The corresponding high-pass filter coefficients are calculated using the following relation:

$$g(n) = (-1)^k h(N-n) (3)$$

TABLE I Low and High-pass Daub-4 Filter Coefficients.



| | | | |
|---|---|---|---|
| h(0) | 0.4829629131 | h(1) | 0.8365163037 |
| h(2) | 0.2241438680 | h(3) | -0.129409522 |
| g(0) | -0.129409522 | g(1) | -0.224143868 |
| g(2) | 0.836516303 | g(3) | -0.482962913 |

Where, h(n) and g(n) are, respectively, the low and high-pass filter coefficients are given in table I. N is the filter order. Equation can be rewritten four-tap FIR filter as:

$$Y_h[k] = [h(0) + h(1)Z^{-1} + h(2)Z^{-2}h(3)Z^{-3}]\, X(n) \qquad (4)$$

$$Y_l[k] = [g(0) + g(1)Z^{-1} + g(2)Z^{-2}g(3)Z^{-3}]\, X(n) \qquad (5)$$

where$Z^{-1}$ operator represents one sample delay in Z-domain.

## IV. PROPOSE ARCHITECTURE

In this paper, the original signal X[n] has N- sample points, is passed through 1×2 demultipler. When select line is 0 then we get even sample and when select line is 1 then we get odd sample. After that we have passed these samples through multiplierdesign based low-pass filter, same process with high-pass filter.Now we get N/2 sample s at the first decomposition level output of multiplier design based high-pass ($Y_H$) and low-pass filter ($Y_L$).

$$Y_L = X(n)h(0) + X(n-1)h(1) + X(n-2)h(2) + X(n-3)h(3) \qquad (6)$$

$$Y_H = X(n)g(0) + X(n-1)g(1) + X(n-2)h(2) + X(n-3)g(3) \qquad (7)$$

At the second decomposition level, the output of multiplier design based low-pass and high-pass filter passed through a register unit.Now the output of register unit passed throughmux. When the select line 0, we get multiplier design based low-pass filter output and when the select line 1, we get multiplier design based high-pass filter.Now we have passed mux output through multiplier design based low-pass filter then we get $Y_{LL}$&$Y_{LH}$ output now same process applied with the multiplier design based high-pass filter we get $Y_{HL}$&$Y_{HH}$.

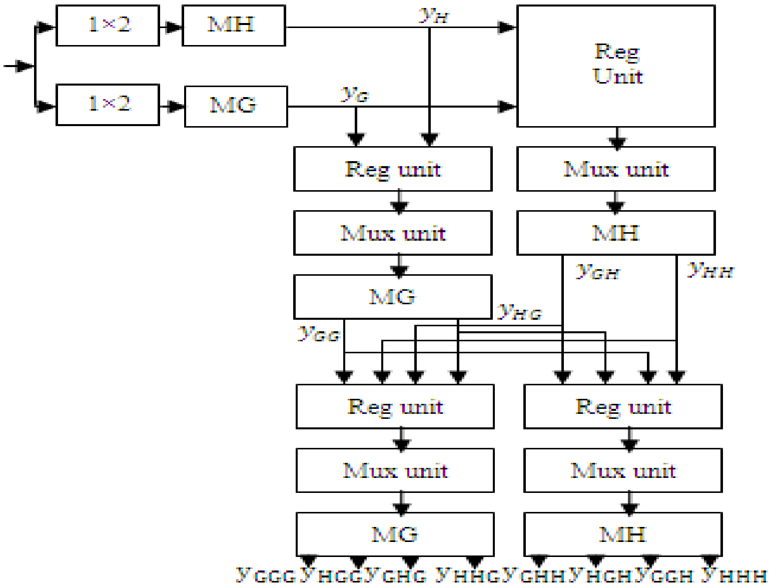


**Figure 2**: 3-Level Multiplier Design based DWPT, MG and MH Means the Multiplier Design Based Low & High-pass Filter.

Select line = 0

$$Y_{LL} = mx(n)h(0)+mx(n-1)h(1)+mx(n-2)h(2)+mx(n-3)h(3)\ (8)$$

$$Y_{LH} = mx(n)g(0)+mx(n-1)g(1)+mx(n-2)h(2)+mx(n-3)g(3)(9)$$

Select line = 1
$Y_{HL}$= mx(n)h(0)+mx(n-1)h(1)+mx(n-2)h(2)+mx(n-3)h(3) (10)

$Y_{HH}$= mx(n)g(0)+mx(n-1)g(1)+mx(n-2)h(2)+mx(n-3)g(3)(11)
Where
mx (n) = mux output (2×1)

At the third decomposition level, the time period is doubled and frequency will be half, and the output of multiplier design based low-pass and high-pass filter is passed through a register unit. Now the output of register unit is passed through mux. When the select line is 00, we get multiplier design based low-pass filter output $Y_{LL}$, the select line is 01, we get$Y_{LH}$ , the select line is 10 we get $Y_{HL}$ and the select line is 11 we get$Y_{HH}$. Now finally we have passed mux output through multiplier design based low pass filter and high pass filter we get $Y_{LLL}, Y_{LHL}, Y_{HLL}, Y_{HHL}$ and $Y_{LLH}, Y_{LHH}, Y_{HLH}, Y_{HHH}$.

Select line = 00

$Y_{LLL}$=mu(n)h(0)+mu(n-1)h(1)+mu(n-2)h(2)+mu(n-3)h(3) (12)

$Y_{LLH}$=mu(n)g(0)+mu(n-1)g(1)+mu(n-2)h(2)+mu(n-3)g(3)(13)

Select line = 01

$Y_{LHL}$=mu(n)h(0)+mu(n-1)h(1)+mu(n-2)h(2)+mu(n-3)h(3) (14)

$Y_{LHH}$=mu(n)g(0)+mu(n-1)g(1)+mu(n-2)h(2)+mu(n-3)g(3) (15)

Select line = 10

$Y_{HLL}$=mu(n)h(0)+mu(n-1)h(1)+mu(n-2)h(2)+mu(n-3)h(3) (16)

$Y_{HLH}$=mu(n)g(0)+mu(n-1)g(1)+mu(n-2)h(2)+mu(n-3)g(3) (17)

Select line = 11
$Y_{HHL}$=mu(n)h(0)+mu(n-1)h(1)+mu(n-2)h(2)+mu(n-3)h(3) (18)

$Y_{HHH}$=mu(n)g(0)+mu(n-1)g(1)+mu(n-2)h(2)+mu(n-3)g(3) (19)

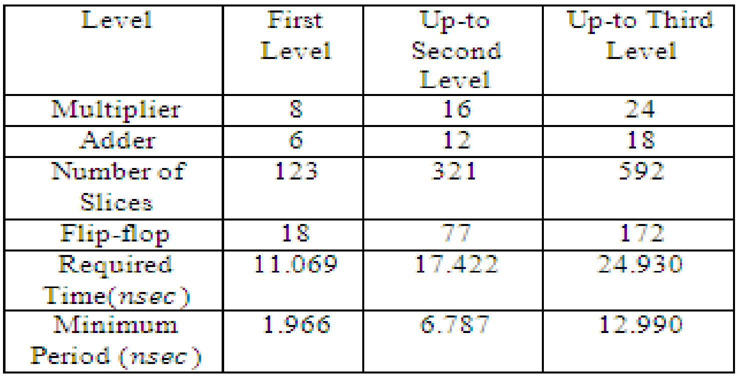
Where
mu(n) = mux output (4×1)

## V. SIMULATION RESULT

We have implemented multiplier design based (MDB) architecture. A comparison between first level, second level and third level multiplier design based architecture for 2-D DWT is given in Table II respectively. This paper provides the clearcut idea in about the application of 8-multiplier and 6-adder in one, two & three level of architecture. In this paper up to second level multiplier design based architecture used in 16 multiplier and 12 adder and also used in third level multiplier design based architecture used in 24 multiplier and 18 adder.

Implementing the proposed multiplier design based up to third decomposition level architecture for DWT has been captured by VHDL and the functionality is verified by RTL and gate level simulation. To estimate the number of slices, flip flop, required time and minimum period information for ASIC design, we have used Xilinx Design Compiler to synthesize the design into gate level. Comparison of practical result up to third decomposition level architecture for 2-D DWT is given in Table II respectively.

TABLE II Comparison betweenFirst Level, Second Level and Third Level Multiplier Design Based architecture for 2-D DWT.



| Level | First Level | Up-to Second Level | Up-to Third Level |
|---|---|---|---|
| Multiplier | 8 | 16 | 24 |
| Adder | 6 | 12 | 18 |
| Number of Slices | 123 | 321 | 592 |
| Flip-flop | 18 | 77 | 172 |
| Required Time($nsec$) | 11.069 | 17.422 | 24.930 |
| Minimum Period ($nsec$) | 1.966 | 6.787 | 12.990 |

## VI. CONCLUSION

In this paper we have proposed multiplier design based (MDB) architecture for 2-D Discrete Wavelet transforms (DWT).

Low pass filter is the average between two sample and high pass filter is the difference between two samples. There is no on-chip memory and memory access during the computation, so that can achieve significant reduction in both die area and power dissipation.

The VHDL language supports these modeling needs at the algorithm or behavioral level, and at the implementation or structural level. It provides a versatile set of description facilities to model DSP circuits from the system level to the gate level. At the system level we can build behavioral models to describe algorithms and architectures.

In this paper architecture is suitable for high speed on-line applications. With this architecture the speed of the wavelet packet transforms is increased, occupied areas of the circuit is reduced about 50% in the previous convolution based architecture and reduces the power about 15-25% in the previous convolution based architecture. It has 100% hardware utilization efficiency.

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