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Temperature Effects On The Hydrogen Content And Passivation Of Silicon Surface Coated With Sio_2 And Sin Films

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Abstract: - A detailed comparison of the passivation quality and its dependence on the low and high temperature anneals has been carried out for various promising Si surface passivation schemes. The passivation schemes investigated include; conventional furnace oxide (CFO) rapid thermal oxide (RTO), belt line oxide (BLO), plasma deposited oxide (PDO), SiN deposited by plasma enhanced chemical vapour deposition (PECVD). The passivated low resistivity (1Ω-cm) p-type silicon samples were subjected to three annealing treatments; 400^{o}C in forming gas (FGA), 730^o in air and 850^{o}C in air to stimulate heat-treatments which were typically used for contact anneal, font ohmic contacts, and back surface field formation respectively for screen printed silicon solar cells. It was found that the passivation quality of PDO, SiN, RTO and CFO single layers improved significantly after the 400^{o}C FGA and 730^o thermal cycles with RTO resulting in the lowest surface recombination velocities (S_{eff}) of 154 and 405 cm/s, respectively. Silicon wafers coated with belt oxide (BLO and BLO/SiN) did not show any improvement in (S_{eff}) which remained at 5000cm/s due to the inferior quality of BLO formed compressed air. The oxide/nitride stack passivation was found to be far superior to single-layer passivation resulting in (S_{eff}) of 70cm/s for the RTO/SiN scheme after the two high temperature anneals (850 and 730^{o}C). A combination of reduced hydrogen content and very low S_{eff} in the RTO/SiN stack suggested that the release of hydrogen from SiN during the anneal further passivated the RTO/Si interface underneath.

Key words: - *Temperature effect, hydrogen content, passivation, Si-SiO_2 and Si-SiN*

I. INTRODUCTION

Screen printed (SP) contact technology is simple, low cost, and manufacturable but screen printed Silicon solar cell efficiency is low due to inherent loss mechanism (Nijis et al, 1994 and Dashi et al, 1996). In order to improve the efficiency of the SP cells, the losses due to higher grid line shading, contact resistance, heavily doped emitter, and very high back surface recombination velocity due to the full metal back, must be minimised. Since the back surface recombination can increase the dark saturation current density of solar cells, the application of an effective back surface passivation could significantly improve the cell performance; this would require a reduction in the back metal coverage coupled with excellent passivation of the non contacted regions at the back.

In addition, as thinner materials are used to reduce the cost, the back-side recombination could have an even bigger impact on the cell performance. Figure 1 shows that, if a metal grid is used on the back with the non contacted back surface fully passivated to produce an S_{eff} of 100cm/s, a thinner photovoltaic (PV) grade material with low minority carrier lifetimes (100μs) could actually produce higher efficiency cells compared to thick cells. This provided the motivation for investigating the low cost manufacturable back passivation schemes subjected to SP solar cell processing steps. The SP solar cell processing steps. The SP solar cell processing involves a 2 min back surface field (BSF) formation at 850^o followed by a 730^{o}C front contact firing for 30s and a 20min forming gas anneal at 400^{o}C.

II. EXPERIMENTAL

1Ω-cm, chemically polished † -type (100), float zone (FZ) wafers were used as substrates which were cleaned in 1:1:2 H_2SO_4: H_2O_2: H_2O for 5 min followed by a 3 min rinse in deionized (DI) water. This was followed by a clean in 1:1:2 HCl: H_2O_2: H_2O for 5 min and a 3 min rinse in D1 water rinse. The thin oxides (100Å) were grown by RTP, BLP and CFP. In addition, PECVD SiO_2 or PDO was deposited at 250^{o}C with 20W power while another set of oxidized samples were coated with PECVD SiN at 300^{o}C with 30W power to form the oxide/nitride stacks. One RTO/SiN sample was coated with 900Å of PDO to form a double-layer AR coating. The quality of each passivation scheme was assessed by determining surface recombination velocity (SRV) by the transient photoconductive decay (PCD) technique. The effective PCD lifetime of the minority carriers was converted to an effective surface recombination velocity (S_{eff}) according to Schroder, (1997)

$$\frac{1}{T_{eff}} = \frac{1}{T_b} + \frac{2S}{W}\frac{a}{} \quad (1)$$

Where T_{eff} is the effective minority carrier lifetime, T_b is the bulk minority carrier lifetime, S is the effective surface recombination velocity, and W is the wafer thickness.
Since FZ wafers had bulk lifetime (T_b) in excess of 1ms, the value of S_{eff} in this study was determined by

$$\frac{1}{T_{eff}} = \frac{2S}{W} \qquad (1)$$

which is valid for very high or infinite carrier lifetime and good SRV (Schroder 1997). Thus, the S_{eff} values represents a maximum or worst case scenario. All the effective minority carrier lifetimes were measured in the low level injection regime between 2×10^{14} and 1×10^{15}.

Measurements were performed at room temperature to determine the hydrogen content of various passivation schemes. The samples analysed by these measurements included (i) SiN without anneal, after forming gas anneal (FGA) at 400°C and after belt line furnace anneals at 730 and 850°C in air (ii) RTO/SiN stack without anneal at 730°C and 850°C in air.

III. GROWN SINGLE LAYER AND STACK PASSIVATION

The S_{eff} for all the single-layer oxides, without anneal, was found to be high, ranging from 550 to 570cm/s for RTO and CFO, respectively and 5000cm/s each, for BLO, PDO and SiN. The very high S_{eff} for PDO and SiN was attributed to very high D_{it} at the dielectric/Si interface due to the damage caused by the reacting species during deposition. High S_{eff} for BLO was due to the poor S_i/S_iO_2 interface formed in the air instead of pure oxygen. Relatively lower S_{eff} for the RTO and CFO suggestd a higher quality interface between RTO/Si and CFO/Si. For the stack passivation schemes, S_{eff} was found to decrease with SiN deposition on most thin S_iO_2 layers with S_{eff} of 167cm/s for RTO/SiN stack.

IV. EFFECT OF 400°C FGA ON SINGLE-LAYER AND STACK PASSIVATION SCHEMES.

Here the low temperature forming gas anneal (FGA) at 400°C for 20min often used to anneal contacts in solar cells, improved the passivation quality of all the passivation schemes except for BLO. For example, the effective surface recombination velocity, for RTO alone decreased from 550 to 154cm/s after the 400°C anneal. There were some improvements in both the CFO and PDO due to the FGA – induced hydrogen passivation of the interface.

On stack passivation, the effective surface recombination velocity of BLO/SiN stack remained very high (>4000cm/s) after FGA. A significant improvement was obtained in the RTO/PDO and RTO + FGA passivation indicating that PDO deposition does not hurt RTO/Si interface underneath. The RTO/SiN and CFO.SiN_o also showed a further reduction in S_{eff} when annealed in forming gas with the S_iN cap resulting in S_{eff} values of 68 and 70cm/s respectively. The reduction in S_{eff} with forming gas anneal was consistent with the observation of other researchers such as Lauinger et al 1995, Narasimha and Rohatgi, 1998.

V. EFFECT OF 730°C ANNEAL ON SINGLE-LAYER AND STACK PASSIVATION SCHEMES

The 730°C in a belt lamp furnace improved the passivation quality of all the passivation schemes except BLo, which remained unchanged. The S_{eff} of PDO, RTO and CFO single layers decreased by a factor of about 2.7, 1.4 and 1.4 respectively, after the 730°C/30s anneal. The SiN single layer showed improvement by a factor of five (from 5000 to 676cm/s) due to the passivation of the SiN/Si interface by the release of a significant amount of hydrogen from SiN film.

The passivation efficiency of RTO/PDO stack improved due to the 730°C anneal resulting in S_{eff} of 451cm/s. The BLO/S-iN passivation scheme showed a marginal improvement due to the extremely poor BLO/Si interface, which could not be revived by hydrogen injection. On the other hand, the PDO/S-iN, CFO/SiN RTO/SiN passivation schemes showed a reduction in S_{eff} values by a factor of 9, 5 and 3 respectively, as a result of the 730°C contact anneal. The decrease in SRV was the result of the release of hydrogen from the SiN coupled with the hydrogen passivation at the RTO/Si interface.

VI. EFFECT OF 850°C ANNEAL ON STACK PASSIVATION

The quality of CFO/SiN and RTO/SiN were found to be superior to all other passivation schemes in this study after the 400°C FGA and 730°C anneals; which mimic the contact anneal and SP contact firing cycles. However, they also need to withstand the AI BSF formation step, which involves 850°C/2 min anneal. Therefore these two stacks were subjected to 850°C anneals. 850°C/2min anneal of CFO/SiN resulted in an S_{eff} value of 102 and 81cm/s for RTO/SiN stack. These two values are impressive and compatible with achieving high efficiency cells on this PV grade materials.

VII. EFFECT OF ANNEALING TIME ON STACK PASSIVATION

Since CFO/SiN and RTO/SiN schemes provided better passivation of the silicon surface after the short high temperature anneal, a study was conducted to see the effects of annealing time. The 730^{o}C/30s anneal on RTO/SiN stack resulted in a very low S_{eff} value of 12cm/s, which increased fourfold when the annealing time was increased to 2 min. Also, the CFO/SiN stack after 730^{o}C/30s anneal resulted in S_{eff} value of 23cm/s and increased twofold as the annealing time increased to 120s. The S_{eff} for RTO/SiN annealed at 850^{o}C increased from 30 to 81cm/s when the annealing time was increased from 30 to 120s. The CFO/SiN stack passivation showed the same trend with S_{eff} varying from 30 to 102cm/s as the 850^{o}C annealing time was increased from 30 to 120s. This suggests that out-diffusion of the hydrogen from the oxide/Si interface as the annealing time increases results in reduction in the passivation quality. Again, it is important to recognise that even though the stack passivation degrades with annealing temperature and time, the final values of $\leq$ 100cm/s are extremely good for high efficiency solar cells.

VIII. CONCLUSION

The passivation quality of various promising dielectric passivation schemes for low resistivity silicon wafer has been compared. Passivation quality is assessed in terms of SRV before and after 400/30min FGA and 730 and 850^{o}C anneals in air. These processes are commonly used for contact anneal, front grid and AI BSF formation of SP solar cells. In addition to single-layer, oxide and nitride films, oxide/nitride stacks are also formed by depositing SiN films on top of thin oxide films to provide antireflection coating for solar cells. In this study it was also found that stack passivation was superior to the counterpart individual films. Higher temperature and longer annealing time could degrade passivation quality. However, by choosing appropriate films and annealing conditions, one could achieve very good surface passivation below 100cm/s on 1Ω-cm p-type silicon. It was found that 400^{o}C/20min anneal improved the passivation quality of all the films. Likewise 730 and 850^{o}C anneals improve passivation, but the best results were obtained for a shorter anneal time in the order of 30s. Unlike the other passivation schemes, the RTO/SiN stack was not only able to withstand 850^{o}C/2min anneal but was actually improved as a result of that. This is because the hydrogen released from the SiN, during this anneal, passivates the RTO/Si interface.

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