

MITIGATION OF HARMONICS IN INVERTER

Ankita Papriwal¹, Dr. Amita Mahor²

Ankita Papriwal¹, P.G. Scholer, NIIST, Bhopal (M.P.), INDIA

Dr. Amita Mahor², H.O.D., Electrical & Electronics Department, NIIST, Bhopal (M.P.), INDIA

Abstract—In recent years power electronic converters are widely used in industrial as well as domestic applications for the control of power flow for automation and energy efficiency. Most of the time these converters draw harmonic current and reactive power from AC source and causes the power quality problems. Recently multilevel power conversion technology has been a very rapidly growing area of power electronics with good potential for further developments. For a multilevel inverter, switching angles at fundamental frequency are obtained by solving the selective harmonic elimination equations in such a way that the fundamental voltage is obtained as desired and certain lower order harmonics are eliminated. The most attractive applications of this technology are in the medium to high-voltage range. Multilevel inverters have many advantages such as low power dissipation on power switches, low harmonic and low electromagnetic interference (EMI) outputs. This paper provides a concise review on multilevel inverter and different levels of cascaded H-Bridge connection.

Key Words— Harmonic suppression, Multilevel Inverter, Total Harmonic Distortion.

I. INTRODUCTION:

Power Electronics inverters are becoming popular for various industrial drive applications. In recent year, inverter have been become necessity for many implementations such as motor controlling & power system.

The term harmonics referred to Power quality in ideal world would mean how pure the voltage is, how pure the current waveform is in its sinusoidal form Power quality is very important to commercial and industrial power system designs. Ideally, the electrical supply should be a perfect sinusoidal waveform without any kind of distortion. If the current or voltage waveforms are distorted from its ideal form it will be termed as harmonic distortion. This harmonic distortion could result because of many reasons. In today's world, prime importance is to derive a method to reduce the harmonic distortion.

Jinghua et al. introduced a general multilevel hybrid topology for 5-level inverter which standardizes and enrich the hybrid multilevel inverter topologies.

Tehrani et al. suggested a novel multilevel inverter model and in this model output voltage waveform for 2, 3, 4 and 5 level are studied and its harmonic content with a low switching frequency is improved, and also this model has very small total harmonic distortion and besides a decrease in cost in comparison with a multilevel inverter classic NPC.

After this **Chen et al.**, presented a novel multilevel inverter topology with no clamping diodes and flying capacitors and this is achieved by extending a two-level phase leg to five level phase leg with self voltage balancing. He suggested this novel topology is more suitable for medium voltage applications with low THD requirements.

After this **Colak et al.** developed a robustly designed inverter block with mathematical model for SPWM modulator to minimize THD ratios of 5-level cascaded voltage source inverter and compare to other conventional models.

After the 5-level cascaded multilevel inverter **Colak et al.** a three-phase 7-level cascaded multilevel inverter with phase disposition SPWM control has been presented, achieving output signals with high quality and very low THD owing to robustly designed mathematical model of multi-carrier modulator.

The main subject of this paper is compare the symmetrical and the hybrid asymmetrical cascade multilevel inverters with the same number of levels in the output voltage and also compare the THD of the different level.

II. INVERTER

DC to AC inverters is those devices which are used to produce inversion by converting a direct current into an alternating current. DC to AC inverters is such devices whose AC output has magnitude and frequency which is either fixed or variable. In case of DC to AC inverters the output AC voltage can be either single phase or three phases. The magnitude of the AC voltage is from the range of 110-380 V AC while the frequencies are 50 Hz, 60Hz or 400Hz.

2.1 Block Diagram of DC-AC Inverter:

The harmonics can be present in any system where inverters are used. The main aim of using an inverter is to produce an ac output from the dc source. Theoretically the output voltage waveform is expected to be sinusoidal, but in practical terms there is definitely going to be distortions due to harmonics present in the system which results into distorted output waveforms. As a result of this, inverters are used in a system in order to produce output waveforms which are purely sinusoidal and distortion free.

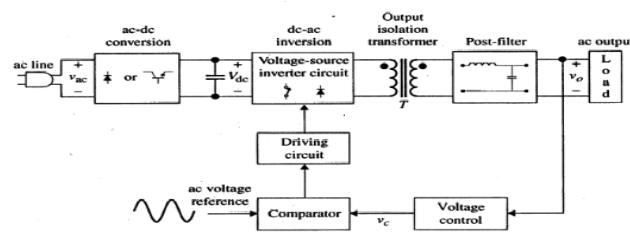


Figure 1: Power Electronic Circuit with DC-AC Inverter.

Figure.1 shows a circuit showing DC-AC inverter along with filters which are used to reduce the effect of harmonics to provide distortion free output ac signal. The front part of the circuit consists of AC to DC converters. These AC to DC converters has one ac frequency i.e. the line frequency and it relies on line communication for switching. The system also consists of DC to AC inverters which are used to turn on or off the power switches. Unlike AC to DC converters in DC to AC inverters, the ac frequency is not the line frequency. The figure also shows a voltage control where variable frequency drives are used to control the speed of motors and provide variable output voltage. Due to this complex structure, the inverter circuits require proper control signals to produce the expected ac output voltage. The figure also shows a filter circuit which is used to reduce the harmonics in the system to produce clean sinusoidal output ac voltage. A comparator circuit is also employed which compares the output ac voltage with the reference ac voltage. If the output ac voltage is more distorted as compared to the reference ac voltage then filter circuits are used again to produce the desired clean sinusoidal AC voltage.

Single Phase Inverters:

There can be many different topologies that can be used for inverter circuits. Inverter circuits are designed differently depending on the way the inverter is intended to be. The figure.2 shows a single phase inverter.

This single phase inverter consists of four IGBT devices (also called power control devices) where two each IGBTs are connected in series with each other.

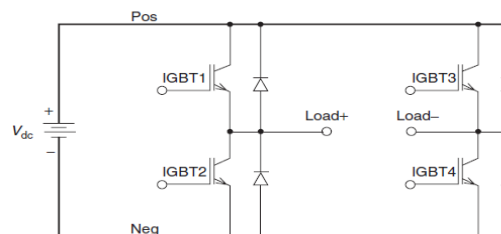


Figure 2: Single Phase Inverter

Three Phase Inverters: Similar to the Single Phase Inverters, the Three Phase Inverters also have different topologies which can be used. Figure.3 shows a three phase inverter circuit.

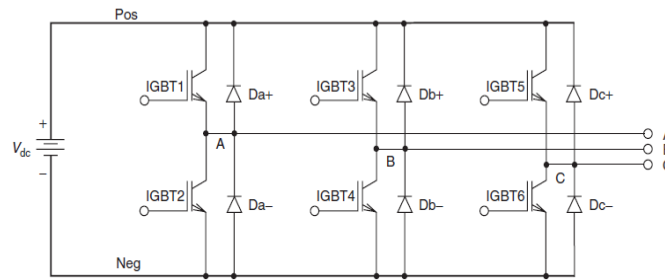


Figure3: Three Phase Inverter.

III. MULTI LEVEL INVERTERS:

In recent years, most industrial application has begun to medium voltage and megawatt power apparatus. It is hard to connect single power semiconductor switch directly to medium voltage & megawatt level. Using two-level inverter cause problem under medium voltage and high power condition. For these reasons, multilevel inverter has emerged as the solution for working with high voltage levels. There are some advantages of multilevel inverter, 1. Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. 2. Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. 3. Multilevel converters can draw input current with low distortion. 4. Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. But there are some Disadvantages of cascaded multilevel inverter

- i) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
- ii) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited.

Multilevel inverters can be implemented using distributed energy resources such as photovoltaic's and fuel cells. Energy storage devices like ultra capacitors and batteries can also be used with multilevel inverters. 2. The multilevel converter can be used as a reactive power compensator can help to improve the power factor of a load. 3. Another possible application of multilevel converters is their use in Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs).

The multilevel inverters are divided in four basic structures: neutral point clamped (NPC), multipoint clamped (MPC), flying capacitor (FC), H-bridge.

Multi level Inverters are a type of inverters whose construction is similar to the single and three phase inverters as explained earlier. The figure.4 shows a multi level inverter which is an extension of single and three phase inverters. Here, four IGBT circuits are connected in three different legs and the diodes are connected in parallel to each leg in opposite direction. Also, the loads are connected between two IGBT circuits for each leg as shown in figure.

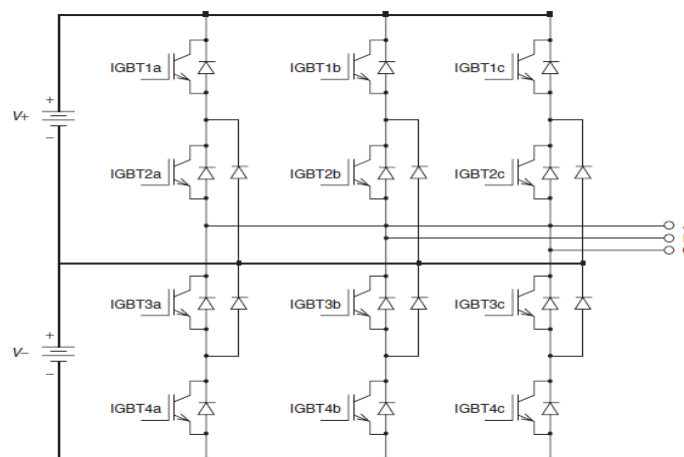


Figure4: Multi level Inverter

3.1 Cascaded H-Bridges Multilevel Inverter (CMLI)

The cascaded H-bridges multilevel inverter is a relatively new inverter structure. A cascaded H-bridges multilevel inverter is simply a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own dc source V_{dc} . By cascading the ac outputs of each H-bridge inverter, an ac voltage waveform is produced.

The number of output phase voltage levels in a cascaded inverter is defined by $m = 2s + 1$

where s is the number of dc sources.

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. Fig.5 shows a general single-phase m -level cascaded inverter. The phase voltage is the sum of each H-bridge outputs and is given as

$$V_{AN} = V_{dc1} + V_{dc2} + V_{dc(s-1)} + V_{dcS}$$

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes $2s+1$. all dc voltage are assumed to be equal, i.e.

$$V_{dc1} = V_{dc2} = \dots = V_{dc(s-1)} = V_{dcS} = V_{dc}$$

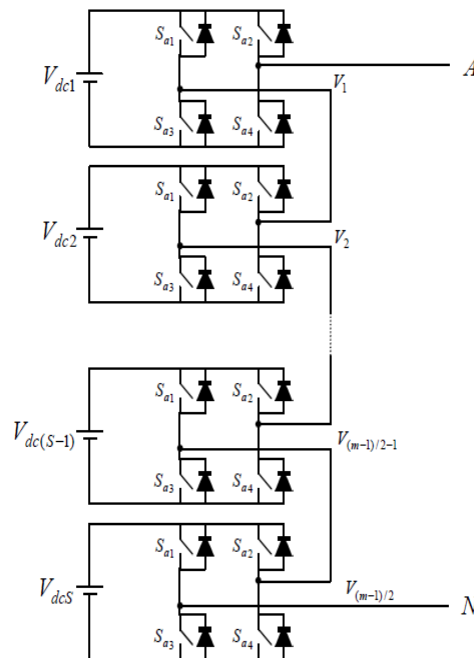


Fig.5 Single Phase Configuration of an m-Level Cascaded Inverter

3.1 Operation of CMLI.

The converter topology is based on the series connection of single-phase inverters with separate dc sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc with five-level and -3Vdc to +3Vdc with seven-level inverter and so on. The staircase waveform is nearly sinusoidal, even without filtering.

The idea of “levels” in a cascaded H-bridges multilevel inverter. A cascaded H-bridges multilevel inverter using s separate dc sources can produce a maximum of $2s + 1$ distinct levels in the output phase voltage.

IV. SIMULATION DESIGNS AND RESULTS

i) Simulation diagram of Single Phase Full Bridge Inverter

(V=100v)

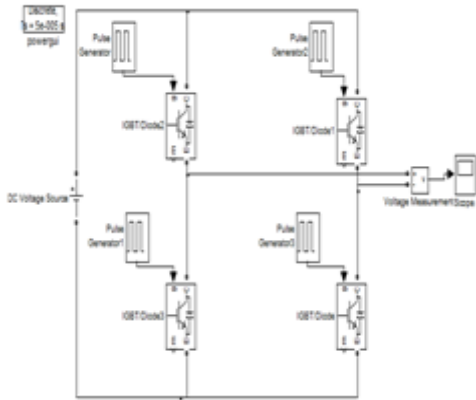


Fig.6 Single Phase Full Bridge Inverter

ii) Simulation diagram of single phase Cascaded H- Bridge 3- level Inverter (Symmetrical dc source V=100V)

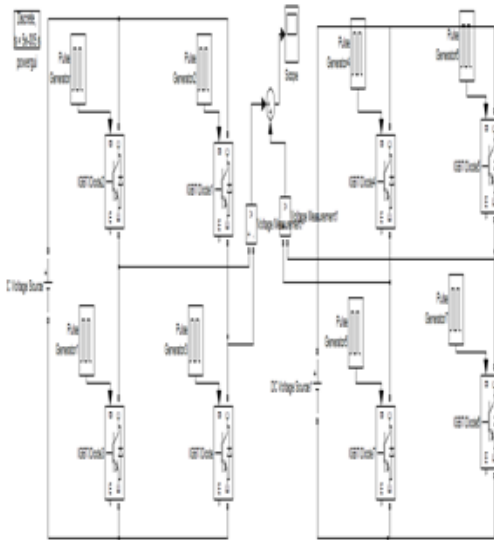


Fig.7 Single Phase Cascaded H- Bridge 3- Level Inverter

ii) Simulation diagram of single phase Cascaded H- Bridge 5- level Inverter (Symmetrical dc source V=100v)

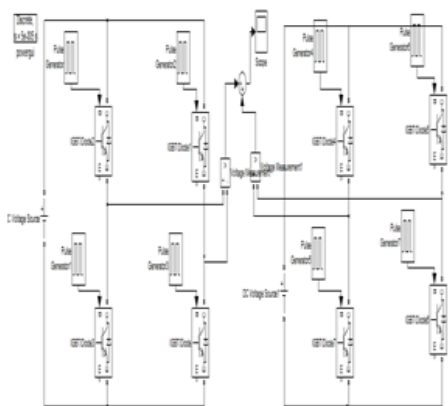


Fig.8. Single Phase Cascaded H- Bridge 5- Level Inverter

ii) Simulation diagram of single phase Cascaded H- Bridge 5- level Inverter (Asymmetrical dc Source $V_1=200v$ $V_2=100v$)

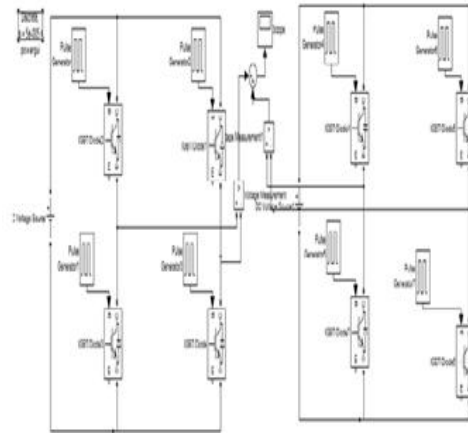


Fig.9. Single Phase Cascaded H- Bridge 5- Level Inverter

WAVEFORMS & RESULTS

i) Waveform of Single Phase Full Bridge Inverter (V=100v)

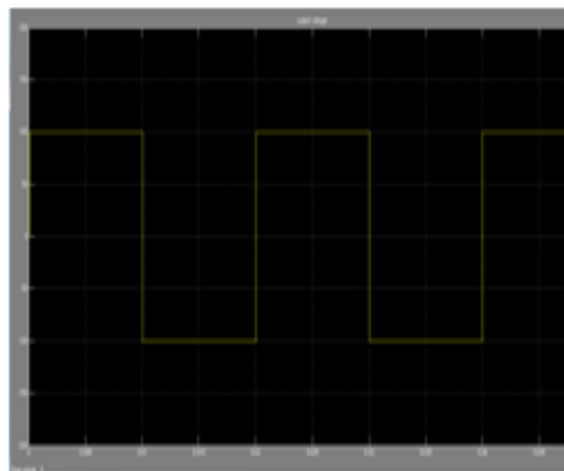


Fig.10 Output Voltage Waveform of Single Phase Full Bridge Inverter

ii) FFT Analysis of Single Phase Full Bridge Inverter (V=100v)

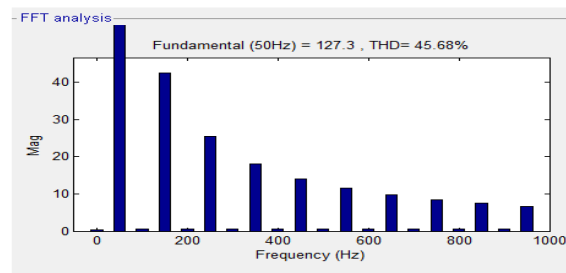


Fig.11 FFT Analysis of Single Phase Full Bridge Inverter

iii) **Waveform of single phase Cascaded H- Bridge 3- level Inverter (Symmetrical dc source V=100V)**

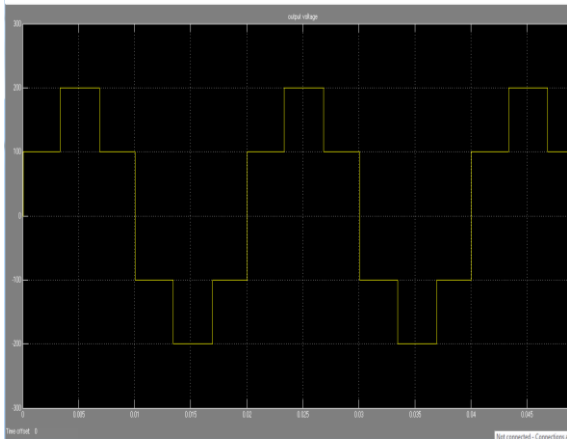


Fig.12 Output Waveform of single phase Cascaded H- Bridge 3- level Inverter

vi) **FFT Analysis of single phase Cascaded H- Bridge 5- level Inverter (Symmetrical dc source V=100V)**

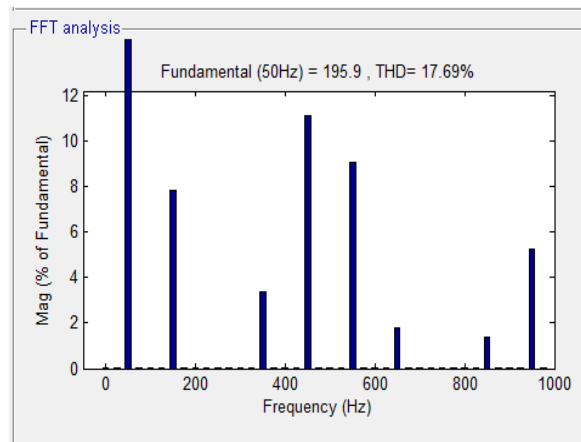


Fig.15 FFT Analysis of single phase Cascaded H- Bridge 5- level Inverter

iv) **FFT Analysis of single phase Cascaded H- Bridge 3- level Inverter (Symmetrical dc source V=100V)**

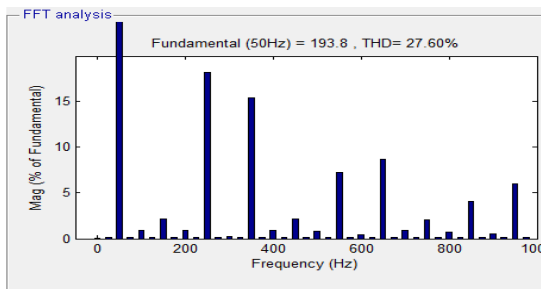


Fig.13 FFT Analysis of single phase Cascaded H- Bridge 3- level Inverter

vii) **Waveform of single phase Cascaded H- Bridge 5- level Inverter (Asymmetrical dc source V₁=200v V₂=100v)**

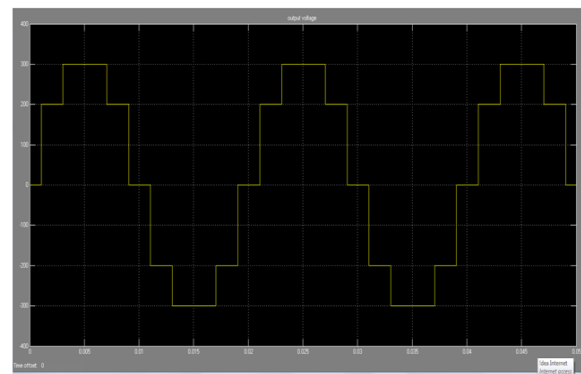


Fig.16 Output Waveform of single phase Cascaded H- Bridge 5- level Inverter

v) **Waveform of single phase Cascaded H- Bridge 5- level Inverter (Symmetrical dc source V=100V)**

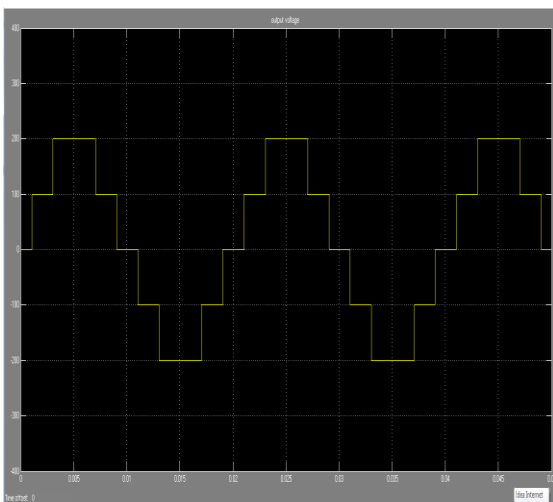


Fig.14 Output Waveform of single phase Cascaded H- Bridge 5- level Inverter

viii) **FFT Analysis of single phase Cascaded H- Bridge 5- level Inverter (Asymmetrical dc source V₁=200v V₂=100v)**

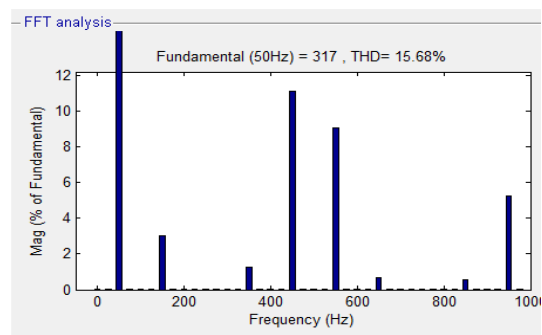


Fig.15 FFT Analysis of single phase Cascaded H- Bridge 5- level Inverter

COMPARISION OF THD ANALYSIS OF m-LEVEL INVERTER

No. Of Levels	3 rd Harmonic %	5 th Harmonic %	7 th Harmonic %	THD %
2- Level	33.34	20	14.29	45.68
3-Level	2.06	18.11	15.36	27.68
5-Level symmetric-al dc source	7.87	0	3.37	17.69
5-Level Asymmetr-ical dc source	3.01	0	1.29	15.68

V. CONCLUSION

The simulation models are successfully designs & results are taken. The main achievement of Cascaded H-Bridge inverter are used for reduction in their total harmonic distortion (THD) and it can be observed that with the increase of level a better fundamental output voltage and minimized total harmonic distortion (THD).

*Two level inverter obtained THD is (45.68%)

*Cascaded H-bridge 3-Level inverter obtained THDS is (27.68%)

*Cascaded H-bridge 5-Level inverter Symmetrical Dc source obtained THDS is (17.69%)

*Cascaded H-bridge 5-Level inverter Symmetrical Dc source obtained THDS is (15.68%)

In the future, the results presented in this paper can also be extended to other hybrid multilevel inverters.

VI. ACKNOWLEDGEMENT

The author would like to thanks to all referees for their useful remarks, which helped to improve the paper. Author's wishing to express cordial thanks to whole Electrical Department of NIIST, Bhopal (M.P.), INDIA for their kind support.

REFERENCES

- [1] Won-Kyo Lee; Soo-Yeol Kim; Jong-Su Yoon; Doo-Hyun Baek; , "A comparison of the carrier-based PWM techniques for voltage balance of flying capacitor in the flying capacitor multilevel inverter," *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE* , vol., no., pp. 6 pp., 19-23 March 2006
- [2] Gupta, R.; Ghosh, A.; Joshi, A.; , "Switching Characterization of Cascaded Multilevel-Inverter-Controlled Systems," *Industrial Electronics, IEEE Transactions on* , vol.55, no.3, pp.1047-1058, March2008
- [3] Fan Zhang; Shuitao Yang; Peng, F.Z.; Zhaoming Qian; , "A zigzag cascaded multilevel inverter topology with self voltage balancing," *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE* , vol., no., pp.1632-1635, 24-28 Feb. 2008
- [4] Zhou Jinghua; Li Zhengxi; , "Research on hybrid modulation strategies based on general hybrid topology of multilevel inverter," *Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008. International Symposium on* , vol., no., pp.784-788, 11-13 June 2008
- [5] Babaei, E.; Hosseini, S.H.; , "New multilevel converter topology with minimum number of gate driver circuits," *Power Electronics, Electrical Drives, Automation and Motion, 2008. SPEEDAM 2008. International Symposium on* , vol., no., pp.792-797, 11-13 June 2008
- [6] Arab Tehrani, K.; Andriatsioharana, H.; Rasoanarivo, I.; Sargos, F.M.; , "A novel multilevel inverter model," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.1688-1693, 15-19 June 2008
- [7] Zambra, D.A.B.; Rech, C.; Goncalves, F.A.S.; Pinheiro, J.R.; , "Power losses analysis and cooling system design of three topologies of multilevel inverters," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.4290-4295, 15-19 June 2008
- [8] Babaei, E.; , "A Cascade Multilevel Converter Topology With Reduced Number of Switches," *Power Electronics, IEEE Transactions on* , vol.23, no.6, pp.2657-2664, Nov. 2008
- [9] Alian Chen; Chenghui Zhang; Hao Ma; Yan Deng; , "A novel multilevel inverter topology with no clamping diodes and flying capacitors," *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE* , vol., no., pp.3184-3187, 10-13 Nov. 2008
- [10] Colak, I.; Kabalci, E.; Bayindir, R.; Sagiroglu, S.; , "The design and analysis of a 5-level cascaded voltage source inverter with low THD," *Power Engineering, Energy and Electrical Drives, 2009. POWERENG '09. International Conference on* , vol., no., pp.575-580, 18-20 March 2009

- [11] Liang Zhou; Smedley, K.; , "Reliability comparison of multi-level inverters for motor drive," *Power & Energy Society General Meeting, 2009. PES '09. IEEE* , vol., no., pp.1-7, 26-30 July 2009
- [12] Farzaneh, A.; Nazarzadeh, J.; , "Precise Loss Calculation in Cascaded Multilevel Inverters," *Computer and Electrical Engineering, 2009. ICCEE '09. Second International Conference on* , vol.2, no., pp.563-568, 28-30 Dec. 2009
- [13] Waware, M.; Agarwal, P.; , "Use of multilevel inverter for elimination of harmonics in high voltage systems," *Computer and Automation Engineering (ICCAE), 2010 The 2nd International Conference on* , vol.2, no., pp.311-315, 26-28 Feb. 2010
- [14] Khomfoi, S.; Praisuwana, N.; Tolbert, L.M.; , "A hybrid cascaded multilevel inverter application for renewable energy resources including a reconfiguration technique," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.3998-4005, 12-16 Sept. 2010
- [15] Colak, I.; Bayindir, R.; Kabcaci, E.; , "Design and analysis of a 7-level cascaded multilevel inverter with dual SDCSs," *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on* , vol., no., pp.180-185, 14-16 June 2010
- [16] Peng, F.Z.; Wei Qian; Dong Cao; , "Recent advances in multilevel converter/inverter topologies and applications," *Power Electronics Conference (IPEC), 2010 International* , vol., no., pp.492-501, 21-24 June 2010
- [17] Hu, Xuefeng; Gong, Chunying; , Xiaolan; xin, Chen; Zhang, Jiayan; , "Analysis of topology and PWM strategy for a new multiple input and multilevel inverter," *Power Electronics for Distributed Generation Systems (PEDG), 2010 2nd IEEE International Symposium on* , vol., no., pp.292-294, 16-18 June 2010
- [18] Ali, R.; Daut, I.; Taib, S.; Jamoshid, N.S.; , "A 5-level multilevel inverter using LM350 voltage regulator IC," *Power Engineering and Optimization Conference (PEOCO), 2010 4th International* , vol., no., pp.137-141, 23-24 June 2010
- [19] Khoucha, F.; Ales, A.; Khoudiri, A.; Marouani, K.; Benbouzid, M.E.H.; Kheloui, A.; , "A 7-level single DC source cascaded H-bridge multilevel inverters control using hybrid modulation," *Electrical Machines (ICEM), 2010 XIX International Conference on* , vol., no., pp.1-5, 6-8 Sept. 2010
- [20] Ahmed, R.A.; Mekhilef, S.; Hew Wooi Ping; , "New multilevel inverter topology with minimum number of switches," *TENCON 2010 - 2010 IEEE Region 10 Conference* , vol., no., pp.1862-1867, 21-24 Nov. 2010
- [21] Deepak, E.S.; Anil, C.S.; Sanjay, S.; Febi, C.; Sajina, K.R.; , "A novel multilevel inverter topology based on multi-winding multi-tapped transformers for improved wave shape requirements," *Power Electronics (IICPE), 2010 India International Conference on* , vol., no., pp.1-5, 28-30 Jan. 2011
- [22] Booma, N.; Sridhar, N.; , "Nine level cascaded H-bridge multilevel DC-link inverter," *Emerging Trends in Electrical and Computer Technology (ICETECT), 2011 International Conference on* , vol., no., pp.315-320, 23-24 March 2011
- [23] Palanivel, P.; Dash, S.S.; , "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *Power Electronics, IET* , vol.4, no.8, pp.951-958, September 2011
- [24] Prasad, K.N.V.; Chellammal, N.; Dash, S.S.; Krishna, A. Murali; Kumar, Y. S Anil; , "Comparison of Photo Voltaic Array based different topologies of cascaded H-bridge multilevel inverter," *Sustainable Energy and Intelligent Systems (SEISCON 2011), International Conference on* , vol., no., pp.110-115, 20-22 July 2011
- [25] Prasad, K.N.V.; Chellammal, N.; Dash, S.S.; Krishna, A. Murali; Kumar, Y. S Anil; , "Comparison of Photo Voltaic Array based different topologies of cascaded H-bridge multilevel inverter," *Sustainable Energy and Intelligent Systems (SEISCON 2011), International Conference on* , vol., no., pp.110-115, 20-22 July 2011
- [26] Manasa, S.; Parimala, R.V.; Chayapathy, V.; , "Advanced pulse width modulation techniques for cascaded multilevel inverters," *Sustainable Energy and Intelligent Systems (SEISCON 2011), International Conference on* , vol., no., pp.259-265, 20-22 July 2011
- [27] Yousefpoor, N.; Fathi, S.H.; Farokhnia, N.; Abyaneh, H.A.; , "THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters," *Industrial Electronics, IEEE Transactions on* , vol.59, no.1, pp.373-380, Jan. 2012
- [28] Ho-Dong Sun; Honnyong Cha; Heung-Geun Kim; Tae-Won Chun; Eui-Cheol Nho; , "Multi-level inverter capable of power factor control with DC link switches," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* , vol., no., pp.1639-1643, 5-9 Feb. 2012
- [29] Kiruthika, C.; Ambika, T.; Seyezhai, R.; , "Implementation of digital control strategy for asymmetric cascaded multilevel inverter," *Computing, Electronics and Electrical Technologies (ICCEET), 2012 International Conference on* , vol., no., pp.295-300, 21-22 March 2012
- [30] Soleimanipour, M.; Goughari, H.S.; Sargolzaei, N.; , "Analysis and Comparison of Multi-level Inverters Based on Two-Level Space Vector PWM," *Computer Modelling and Simulation (UKSim), 2012 UKSim 14th International Conference on* , vol., no., pp.464-469, 28-30 March 2012
- [31] Jamuna, P.; Rajan, C.C.A.; , "MSPWM & MTPWM techniques for asymmetric H-bridge multilevel inverter," *Advances in Engineering, Science and Management (ICAESM), 2012 International Conference on* , vol., no., pp.501-504, 30-31 March 2012
- [32] Gupta, K.K.; Jain, S.; , "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *Power Electronics, IET* , vol.5, no.4, pp.435-446, April 2012
- [33] Najafi, E.; Yatim, A.H.M.; , "Design and Implementation of a New Multilevel Inverter Topology," *Industrial Electronics, IEEE Transactions on* , vol.59, no.11, pp.4148-4154, Nov. 2012