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Performance Evaluation of Multi Carrier Based PWM Techniques for Single Phase Five Level H-Bridge Type FCMLI

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ABSTRACT : - *The Flying Capacitor Multi Level Inverter (FCMLI) has a great advantage with respect to the availability of voltage redundancies. This work proposes a switching pattern for a modified inverter structure. It is used to improve the performance of chosen single phase five level H-bridge type FCMLI as compared to conventional FCMLI. The chosen multi level inverter is simulated for various multicarrier based Pulse Width Modulation(PWM) techniques for a resistive load. The PWM techniques include Phase Disposition (PD) PWM, Phase Opposition and Disposition (POD) PWM, Alternative Opposition and Disposition (APOD) PWM, Carrier Overlapping (CO) PWM, Phase Shift (PS) PWM and Variable Frequency (VF) PWM and the harmonics of the output voltages are observed for various modulation indices. The performance of chosen FCMLI is confirmed through MATLAB-SIMULINK based simulation. It is observed that sinusoidal reference with PODPWM provides output with relatively low distortion. Its also seen that COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage*.

Keywords: *– CF, DF, FCMLI, FF, PSPWM, THD, VF*

I. INTRODUCTION

Power switches with the suitable switching frequency at ratings above 5kV are rare; hence it is difficult to achieve inverter output voltage which is compatible to the medium voltage grid. One approach is to utilize the MLI structure. Multilevel inverter is an array of power semiconductor switches and voltage sources which is switched in a manner that an output voltage of stepped waveform is generated. Several multilevel topologies have evolved: most common are the Diode Clamped Multilevel Inverter (DCMLI), flying-capacitor multilevel inverter and Modular Structured Multilevel Inverter (MSMI). In addition there are emerging multilevel topologies such as the asymmetric hybrid multi level inverters and soft-switching multilevel inverters. Jeon et al [1] introduced a symmetric carrier technique of CRPWM for voltage balance method of flying capacitor multilevel inverter. Boora et al [2] proposed voltage sharing converter to supply single phase asymmetrical four level diode clamped inverter with high power factor loads. Panagis et al [3] have discussed comparison of state of the art multilevel inverters. Tolbert et al [4] have proposed elimination of harmonics in a multilevel converter with nonequal DC sources. Nami et al [5] have presented a hybrid cascade converter topology with series connected symmetrical and asymmetrical diode clamped H-bridge cells. Shanthi and Natarajan [6] have carried out comparative study on carrier overlapping PWM strategies for five level flying capacitor inverter. Porselvi and Muthu [7] have also compared cascaded H-bridge, neutral point clamped and flying capacitor multilevel inverters using multicarrier PWM. Haiwen et al [8] have discussed hybrid cascaded multilevel inverter with PWM control method. Ramani [9] presented switching pattern selection scheme based 11 level flying capacitor multilevel inverter fed induction motor. Shukla et al [10] analyzed flying capacitor multilevel inverter and its applications in series compensation of transmission lines. This literature survey reveals few papers only on various PWM techniques and FCMLI. Hence this work presents a new approach for controlling the harmonics of output voltage of chosen H-bridge type FCMLI fed resistive load employing sinusoidal reference. Simulations are performed using MATLAB-SIMULINK.

II. MULTILEVEL INVERTER

MLIs divide the main DC supply voltage into several DC sources which are used to synthesize an AC voltage from a stepped approximation of the desired sinusoidal waveform. The stepped approximation is also popularly known as the staircase model. The number of stages (cells or capacitors depending on the respective topology) helps decide the power capacity of the converter as a whole. Suitable connections either in series or shunt mode or both are done to achieve higher voltage and/or current ratings. One of the biggest advantages of using a MLI is that the transformer can be eliminated and this helps enhance efficiency and cost effectiveness. Additional features such as its battery management capability, redundant switching states in inverter operation, and scalability make the cascade inverter the MLI of choice.

II. (a) Conventional FCMLI

FCMLI is similar to the Neutral Point Clamped (NPC) topology. Also known as the capacitor-clamped MLI topology it allows more flexibility in waveform synthesis and helps balance voltage across the clamped capacitors. A conventional single phase five level FCMLI topology is shown in Fig.1. One of the biggest advantages of FCMLI over the NPC topology is that one capacitor replaces two diodes (clamping / anti-parallel diodes) resulting in a natural simplification of topology and reduction in overall losses.

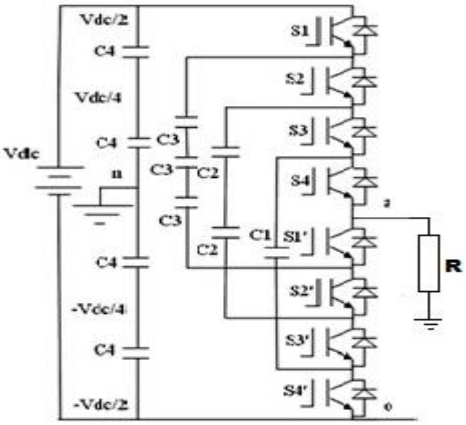

Fig. 1 Conventional single phase five level FCMLI

m-level flying capacitor multilevel inverter has 'm' levels of output voltage. All the capacitors are of equal value; an m-level inverter will require a total of (m-1)×(m-2)/2 clamping capacitors per phase leg in addition to (m-1) main dc bus capacitors. The DC bus consists of four capacitors acting as voltage divider. For a DC bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$ and voltage stress on each device is limited to $V_{dc}/4$ through clamping capacitor. If the voltage of the main DC-link capacitor is Vdc, the voltage of the innermost capacitor clamping the innermost two devices is Vdc/(m-1). The middle point of the four capacitors 'n' can be defined as the neutral point. The numbering order of switches is S1, S2, S3, S4, S1', S2', S3' and S4'. The switches are grouped into four pairs (S1,S1'), (S2,S2'), (S3,S3') and (S4,S4'). Thus if S1 is ON, S1' is OFF and vice-versa. The output voltage V_{an} has five states: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$.

II. (b) Chosen H-bridge type FCMLI

All the clamping capacitors in FCMLI are equal values. The size of the voltage increases between two consecutive legs of the clamping capacitors and hence the size of voltage steps in the output waveform and the elimination of the lower order harmonics. In this paper, a five level symmetrical flying capacitor multilevel inverter uses a modified switching technique in such a way that the number of clamping capacitors is minimized and hence an expected decrease in the converter's switching losses. This topology promises low harmonic distortion and hence there would be no need of filters to provide switch combination redundancy for balancing different voltage levels, Table 1 shows that comparisons of power components used in conventional as well as chosen FCMLI. Fig.2 shows a configuration of single phase five level H-bridge type FCMLI. Here also the same output voltage states exist: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$. To study the operation of the chosen H-bridge type FCMLI, the PWM scheme has been simulated using MATLAB – SIMULINK / POWER SYSTEM BLOCKSET / POWER GUI. The gating pulses for the inverter are generated for various values of modulation index m_a and for various PWM techniques. The simulation results for the different modulation indices with multicarrier SPWM of chosen FCMLI is presented for m_a ranging from 0.6-1.

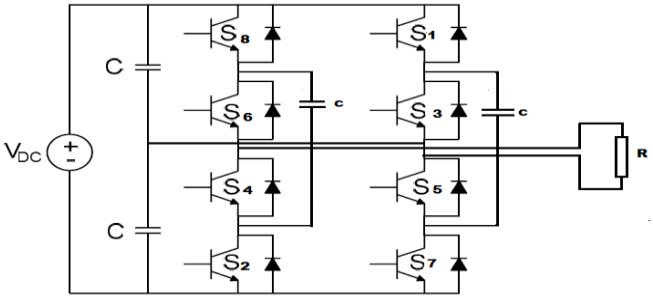

Fig. 2 Chosen single phase H-bridge type five level FCMLI

Table-1 Comparison between conventional and chosen FCMLIs

Type of MLI	Conventional FCMLI	Chosen FCMLI
Main power devices	8	8
Main diodes	8	8
Clamping capacitor	6	2
DC bus capacitors	4	2
No. of leg	1	2

III. INVERTER TOPOLOGY AND SWITCHING STATES

Several modulation strategies have been developed for multilevel inverters. The most common used is the multi carrier sub harmonic PWM technique. The principle of the multicarrier PWM is based on a comparison of a sinusoidal reference waveform with triangular carrier waveforms. m-1 carriers are required to generate m levels. The carriers are in continuous bands around the reference zero. They have the same amplitude A_c and the same frequency f_c. The sine reference waveform has a frequency f_r and A_r is the peak to peak value of the reference waveform. At each instant, the result of the comparison is 1 if the triangular carrier is greater than the reference signal and 0 otherwise. The output of the modulator is the sum of the different comparisons which represents the voltage level. The strategy is therefore characterized by the two following parameters called amplitude modulation index m_a and frequency modulation index m_f:

$$m_f = \frac{f_c}{f_r}$$

The amplitude modulation indices are for

(i) PDPWM, PODPWM, APODPWM and VFPWM: $\frac{2A_r}{(m-1)*A_c}$

(ii) COPWM = $\frac{A_r}{(\frac{m}{4})} * A_c$

(iii) PSPWM = $\frac{A_r}{(\frac{A_c}{2})}$

This paper uses all well known multicarrier based multilevel PWM strategies such as PDPWM, PODPWM, APODPWM, COPWM, PSPWM and VFPWM. Fig.3 shows the sample SIMULINK model developed for PSPWM technique for chosen inverter and Fig.4 shows the sample source block.

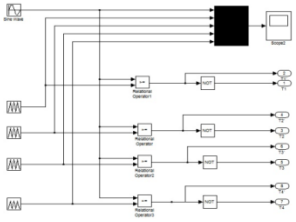

Fig. 3 Sample SIMULINK model developed for chosen single phase inverter for PSPWM technique

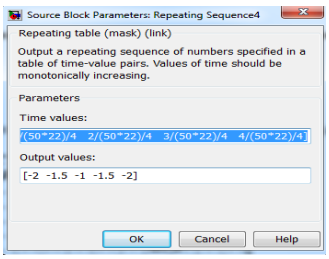

Fig. 4 Sample source block in SIMULINK for triangular carrier.

IV. TYPES OF CARRIER BASED SPWM TECHNIQUES

Sinusoidal PWM can be classified according to carrier and modulating signals. This work used the intersection of a sine wave with a triangular wave to generate firing pulses. There are many alternative strategies to implement this. They are as given below.

Phase Opposition Disposition (POD) PWM where the carriers above the zero reference are in phase but shifted by 180° from those carriers below the zero reference.

Alternative Phase Opposition Disposition (APOD) PWM where each carrier band is shifted by 180° from the adjacent bands.

In Phase Disposition (PD) PWM all the carriers are in phase.

Phase Shift PWM (PSPWM) : all carrier signals have the same amplitude and frequency but they are phase shifted by 90 degrees to each other.

Carrier Overlapping PWM (COPWM): all carriers with the same frequency and same peak to peak amplitude are disposed such that the bands they occupy overlap each other.

Variable Frequency PWM (VFPWM): carriers have the variable frequency and same amplitude each other.

IV. (a) Phase Opposition Disposition (POD) PWM

The rules for phase opposition disposition method for a multilevel inverter are

1) 4 carrier waveforms are arranged as in Fig.5 in phase opposition disposition.
2) The converter is switched to + Vdc/2 when the sine wave is greater than both upper carriers.
3) The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
4) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.
5) The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.
6) The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers.

The above same rule is applicable to all PWM strategy i.e. PD,POD,APOD,CO,PS,VF

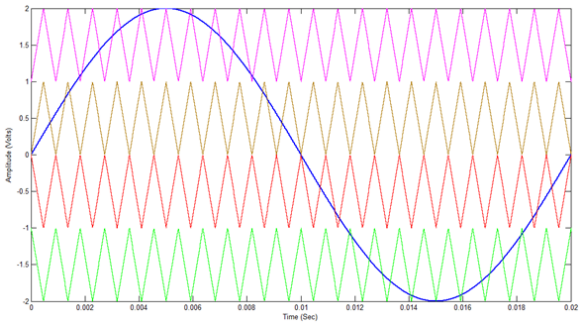

Fig. 5 Carrier arrangement for PODPWM strategy (m_a=0.8 and m_f=22)

IV. (b) Alternative Phase Opposition Disposition (APOD) PWM

This technique requires each of the (m-1) carrier waveforms for an m-level output to be phase displaced from another by 180 degree alternatively as shown in Fig. 6.

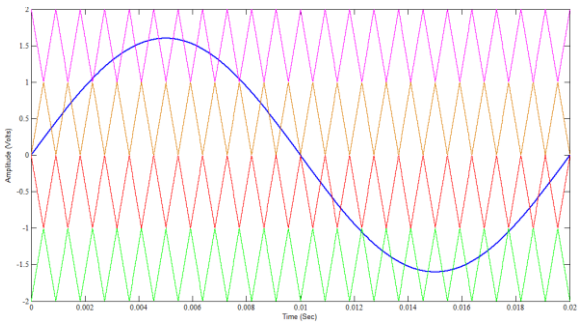

Fig. 6 Carrier arrangement for APODPWM strategy (m_a=0.8 and m_f=22)

IV. (c) Phase Disposition (PD) PWM

This technique is similar to APOD except the carriers are in phase as shown in Fig.7.

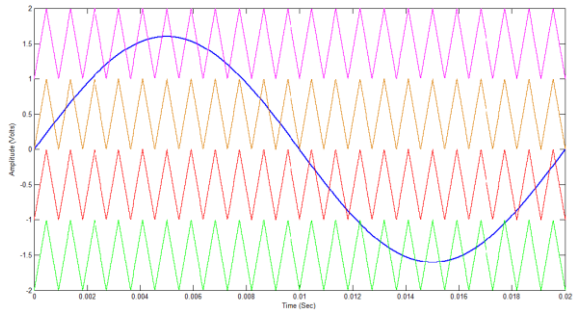

Fig. 7 Carrier arrangement for PDPWM strategy (m_a=0.8 and m_f=22)

IV. (d) Phase Shift PWM (PSPWM)

Number of carriers all of which are appropriately phase shifted are shown in Fig.8.

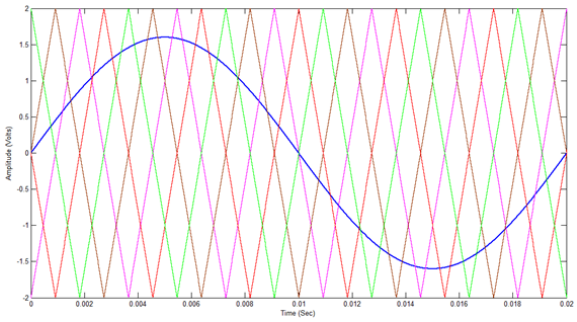

Fig. 8 Carrier arrangement for PSPWM strategy (m_a=0.8 and m_f=22)

IV.(e) Carrier Overlapping PWM (COPWM)

For an m level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to- peak amplitude A_c are disposed such that the bands they occupy overlap each other (Fig.9). The overlapping vertical distance between each carrier is $A_c/2$. The reference waveform has amplitude of A_r and frequency of f_r and it is centered in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off

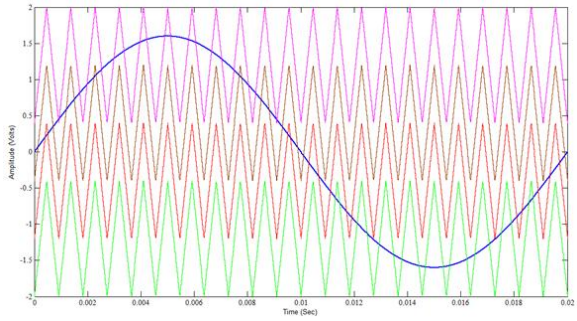

Fig. 9 Carrier arrangement for COPWM strategy (m_a=0.8 and m_f=22)

IV. (f) Variable Frequency (VFPWM)

The number of switching's for upper and lower devices of chosen MLI is much more than that of intermediate switches in PWM using constant frequency carriers. In order to equalize the number of switching's for all the switches, variable frequency PWM strategy is used as illustrated in Fig.10 in which the carrier frequency of the intermediate switches is properly increased to balance the number of switching's for all the switches.

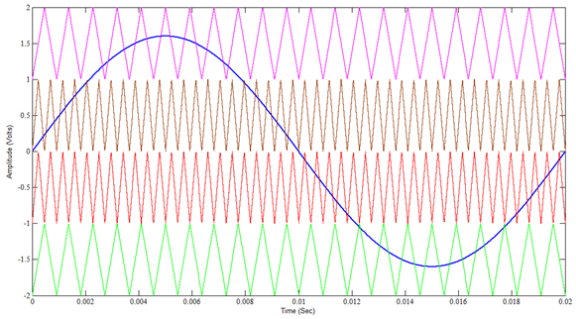

Fig. 10 Carrier arrangement for VFPWM strategy (m_a=0.8 and m_f=22 for upper and lower switches, m_f=44 for intermediate switches)

V. SIMULATION RESULTS

Simulation studies are performed by using MATLAB-SIMULINK to verify the proposed multi carrier based PWM strategies for chosen single phase H- bridge type flying capacitor five level inverter for various values of m_a ranging from 0.6 – 1 and corresponding %THD values are measured using FFT block and they are shown in Table 2. Table 3 shows the V_{RMS} of fundamental of inverter output for the same modulation indices. Figs.11-22 show the simulated output voltages of chosen FCMLI and the corresponding FFT plots with different strategies but only for one sample value of m_a=0.8 and m_f=22. Fig.11 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig.12. from Fig.12, it is observed that the PODPWM strategy produces significant 15th and 17th harmonic energy. Fig.13 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig.14. From Fig.14, it is observed that the APODPWM strategy produces significant 17th and 19th harmonic energy. Fig.15 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig.16. From Fig.16, it is observed that the PDPWM strategy produces significant 12th, 14th 18th and 20th harmonic energy. Fig.17 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig.18. From Fig.18, it is observed that the PSPWM strategy produces significant 11th, 17th and 19th harmonic energy. Fig.19 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig.20. From Fig.20, it is observed that the COPWM strategy produces significant 3rd and 20th harmonic energy. Fig.21 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig.22. From Fig.22, it is observed that the VFPWM strategy produces significant 18th and 20th harmonic energy.

The following parameter values are used for simulation: V_{DC}=440V, fc=1100Hz and R (load) =100 ohms.

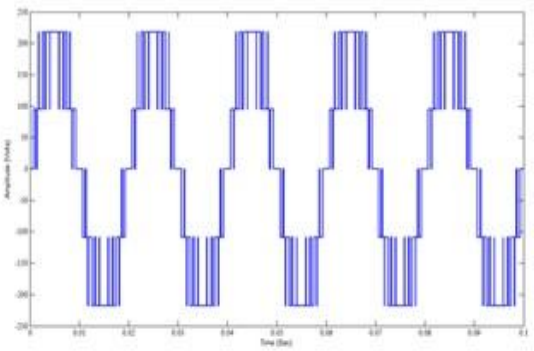

Fig. 11 Simulated five level output voltage generated by PODPWM technique for R load

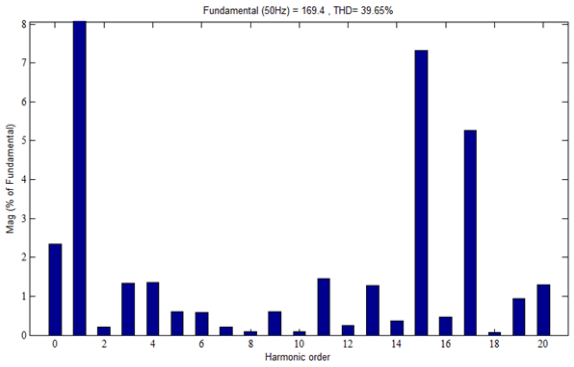

Fig. 12 FFT - harmonic spectrum of output of PODPWM strategy

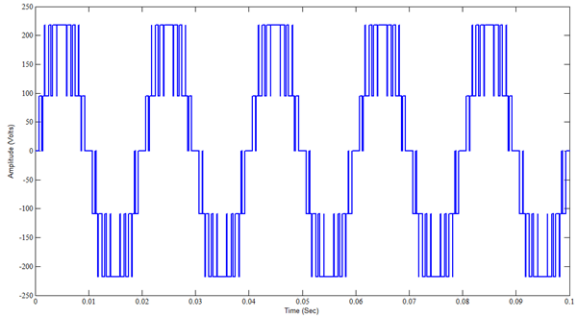

Fig. 13 Simulated five level output voltage generated by APODPWM technique for R load

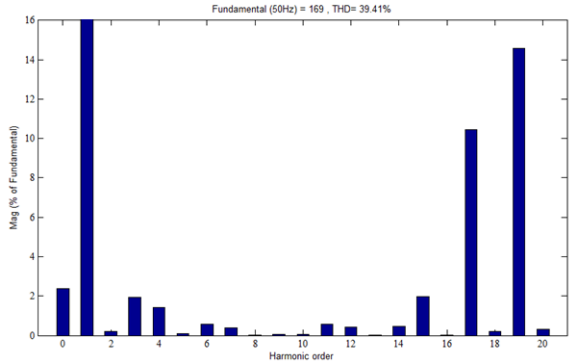

Fig. 14 FFT - harmonic spectrum of output of APODPWM strategy

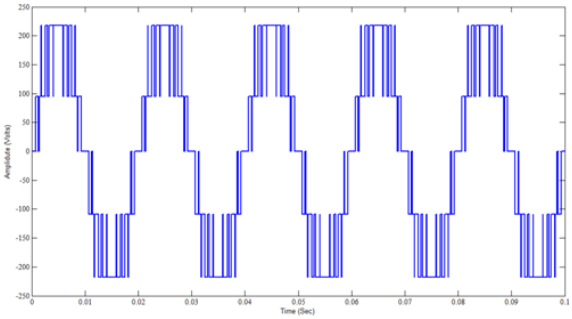

Fig. 15 Simulated five level output voltage generated by PDPWM technique for R load

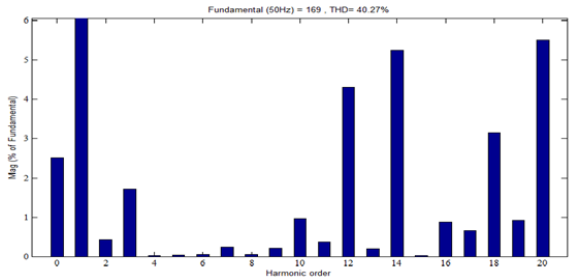

Fig. 16 FFT - harmonic spectrum of output of PDPWM strategy

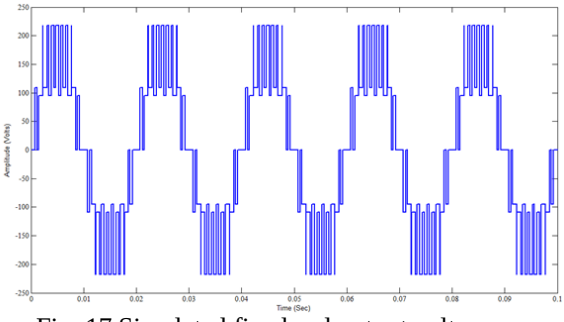

Fig. 17 Simulated five level output voltage generated by PSPWM technique for R load

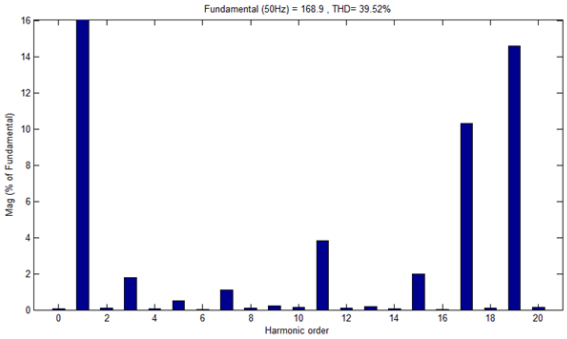

Fig. 18 FFT - harmonic spectrum of output of PSPWM strategy

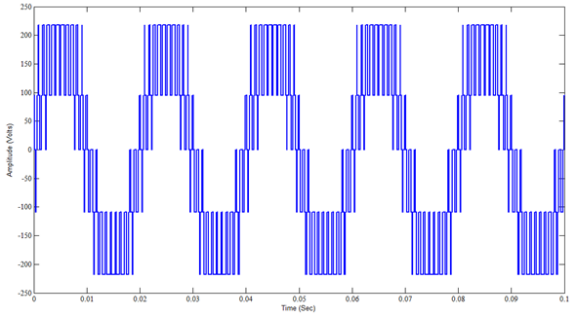

Fig. 19 Simulated five level output voltage generated by COPWM technique for R load

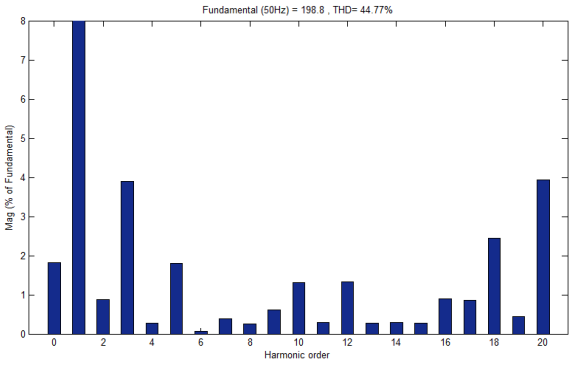

Fig. 20 FFT - harmonic spectrum of output of COPWM strategy

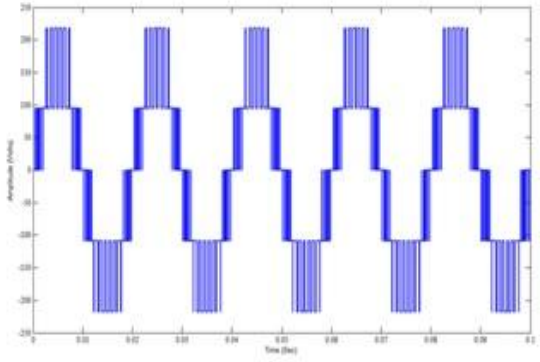

Fig. 21 Simulated five level output voltage generated by VFPWM technique for R load

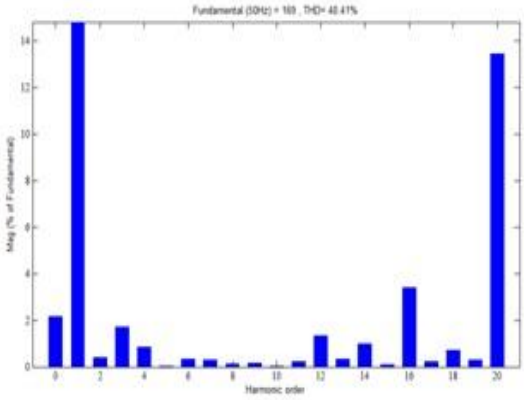

Fig. 22 FFT - harmonic spectrum of output of VFPWM strategy

Table-2
%THD of output voltage for different m_a

m_a	PD	POD	APOD	VF	CO	PS
1	27.91	27.66	27.7	27.94	34.03	27.77
0.9	34.7	34.39	34.94	34.96	39.09	35.03
0.8	40.27	39.65	39.41	40.41	44.77	39.52
0.7	44.05	43.61	43.61	44.1	51.23	43.81
0.6	45.88	44.88	44.52	46.06	60.51	44.84

Table-5
FF of output voltage for different m_a

m_a	PD	POD	APOD	VF	CO	PS
1	81.83	117.6	120.8	101.45	181.88	inf
0.9	72.6	75.95	78.21	62.34	131.63	inf
0.8	67.33	51.19	50.63	55.58	76.83	1990
0.7	30.17	34.2	34.6	32.86	60.81	inf
0.6	23.05	23.6	23.25	11.69	49.69	inf

Table-6
DF of output voltage for different m_a

m_a	PD	POD	APOD	VF	CO	PS
1	0.448	0.333	0.279	0.327	0.765	0.199
0.9	0.425	0.316	0.220	0.286	0.656	0.194
0.8	0.231	0.191	0.248	0.226	0.499	0.212
0.7	0.243	0.302	0.298	0.315	0.292	0.173
0.6	0.265	0.505	0.514	0.411	0.166	0.128

Table-3
V_{RMS} (fundamental) of output voltage for different m_a

m_a	PD	POD	APOD	VF	CO	PS
1	152.2	151.7	152.2	152.2	163.7	152.2
0.9	136	135.2	136.1	135.9	152.7	136.1
0.8	119.5	119.8	119.5	119.5	140.6	119.4
0.7	103.5	103.3	103.8	103.5	127.7	103.8
0.6	87.83	88.3	87.89	87.84	112.8	87.89

Table-4
CF of output voltage for different m_a

m_a	PD	POD	APOD	VF	CO	PS
1	1.414	1.414	1.414	1.414	1.414	1.414
0.9	1.414	1.414	1.414	1.414	1.414	1.414
0.8	1.414	1.414	1.414	1.414	1.414	1.414
0.7	1.414	1.414	1.414	1.414	1.414	1.414
0.6	1.414	1.414	1.414	1.414	1.414	1.414

VI. CONCLUSION

Single phase H-bridge type flying capacitor five level inverter employing different multi carrier single reference modulation schemes has been investigated. It is found from Table 2 that PODPWM technique provides output with relatively low distortion. COPWM technique is observed to perform better since it provides relatively higher fundamental RMS output voltage (Table 3). Table 4 shows crest factor; Table 5 provides FF and Table 6 displays DF for all modulation indices. Appropriate PWM may be employed depending on the performance index required in a chosen application of MLI.

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