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Design of Low-Offset Voltage Dynamic Latched Comparator

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ABSTRACT

The offset voltage of the dynamic latched comparator is analyzed in detailed and dynamic latched comparator design is optimized for the minimal offset- voltage based on the analysis in this paper. As a result offset-voltage was reduced from 0.87µV (in conventional double tail latched comparator) to 0.3µV (in case of proposed comparator. The simulated results of the conventional as well as proposed comparator have been shown on pspice orcad 9.2 versions.

Keywords- *MOSFET, Comparator, Offset Voltage, PSPICE*

INTRODUCTION

Due to low-offset, fast speed, low power consumption ,high input impedance, CMOS dynamic latched comparator are very attractive for many applications such as high speed analog-to-digital convertors(ADCs), memory sense amplifiers(SAs) and data receivers. Scaling is used in CMOS transistor to decrease power consumption and occupying area. Offset-voltage of the comparator exceeds tens mV due to transistor mismatch. In conventional designs, we used pre-amplifiers for offset- voltage cancellation (1) but it increases power consumption due to wide bandwidth amplifier are required to reduce the offset-voltage in the high frequency operation. Furthermore it is very difficult to realize a high voltage gain amplifier because of low drain resistance caused by scaling. Therefore we strongly required a technique to reduce the offset-voltage without using amplifier. In recent years, some offset-voltage cancellation techniques were proposed.

In reference (2), load capacitances used in the comparator are controlled digitally to reduce the offset-voltage. The resolution of the calibration is determined by the size of the load capacitance and the digital word but it gives a high resolution ADC with lower speed and wider area.

In this paper, we have proposed a low-offset latched comparator using new dynamic offset cancellation technique. It has two phases, first one a reset mode and second regenerative mode. Furthermore, due to the input common mode variation, increasing offset-voltage can also be reduced.

CONVENTIONAL CIRCUIT

The mismatch of the transistors threshold voltages is the reason behind the offset-voltage of the comparator. We have taken a conventional double- tail latched comparator circuit as shown in figure (1) and its signal behavior furthermore; offset voltage due to each stage of the conventional comparator is obtained from dc sweep simulation as shown in figure. The comparator circuit is designed using orcad pspice 9.2 version. We have taken aspect ratio W/L=1um/0.065um,conversion frequency fc=500MHz and supply voltage (V_{DD}) =1V.

Second stage offset voltage depends conversion gain G1 between the 1st stage and 2nd stage. By this way the mismatch of the threshold voltage of the input transistors becomes dominant in the offset voltage of the comparator. Therefore offset voltage can be reduced by cancelling the threshold voltage mismatch of the M1 and M2. When we cancel the mismatch threshold voltage of the transistors (M1,M2),2nd stage offset- voltage becomes dominant in the comparator offset-voltage. For that G1 must be kept high to reduce the 2nd stage offset. As shown in figure(3) offset voltage increases from 0.3µV to 0.87µV when Vcmi changes from 0.3V to 0.4V.Therefore we have to design a circuit that can decide G1without being affected by Vcmi.

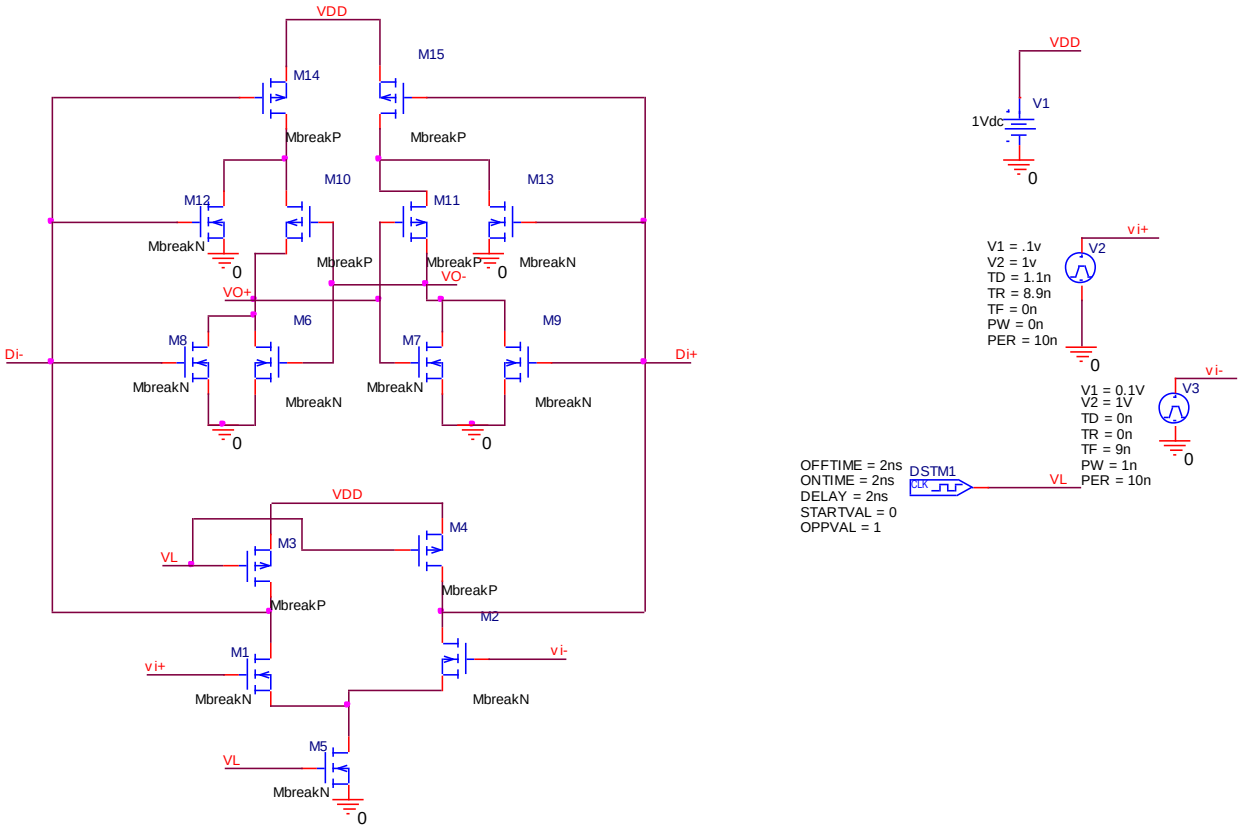

Fig.1. The conventional double-tail latched comparator

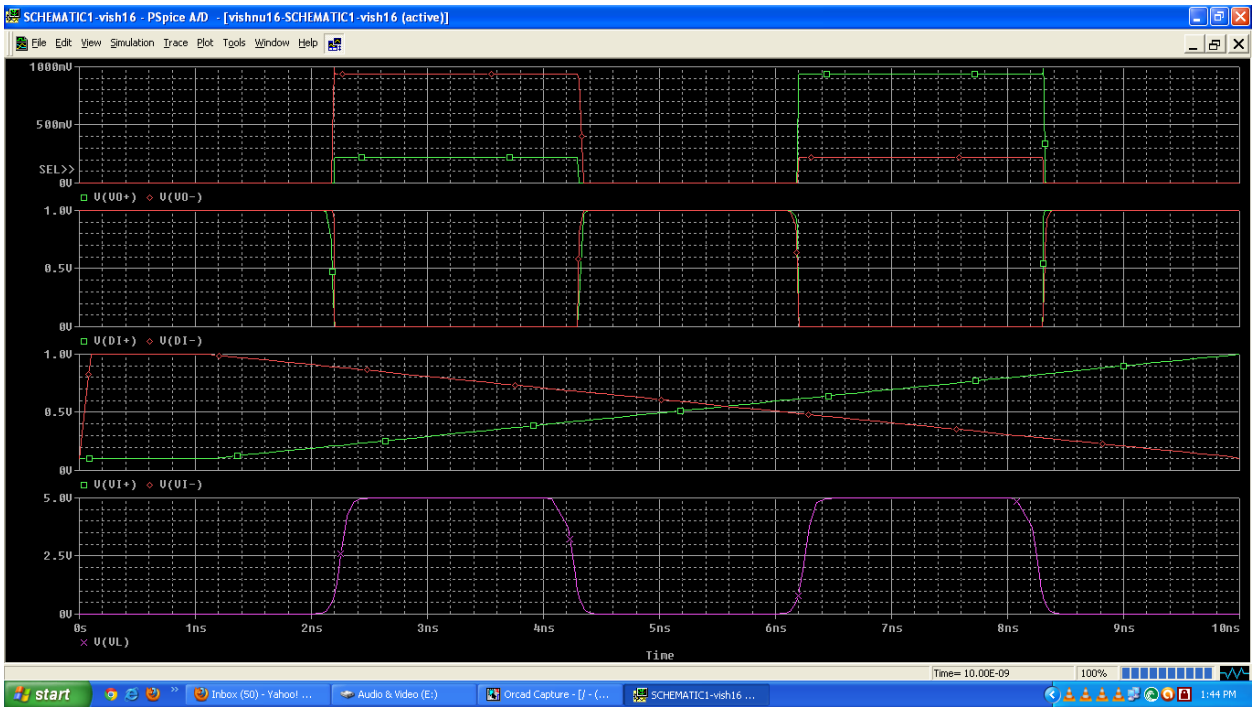

Fig. 2.transient response of Input and output waveform

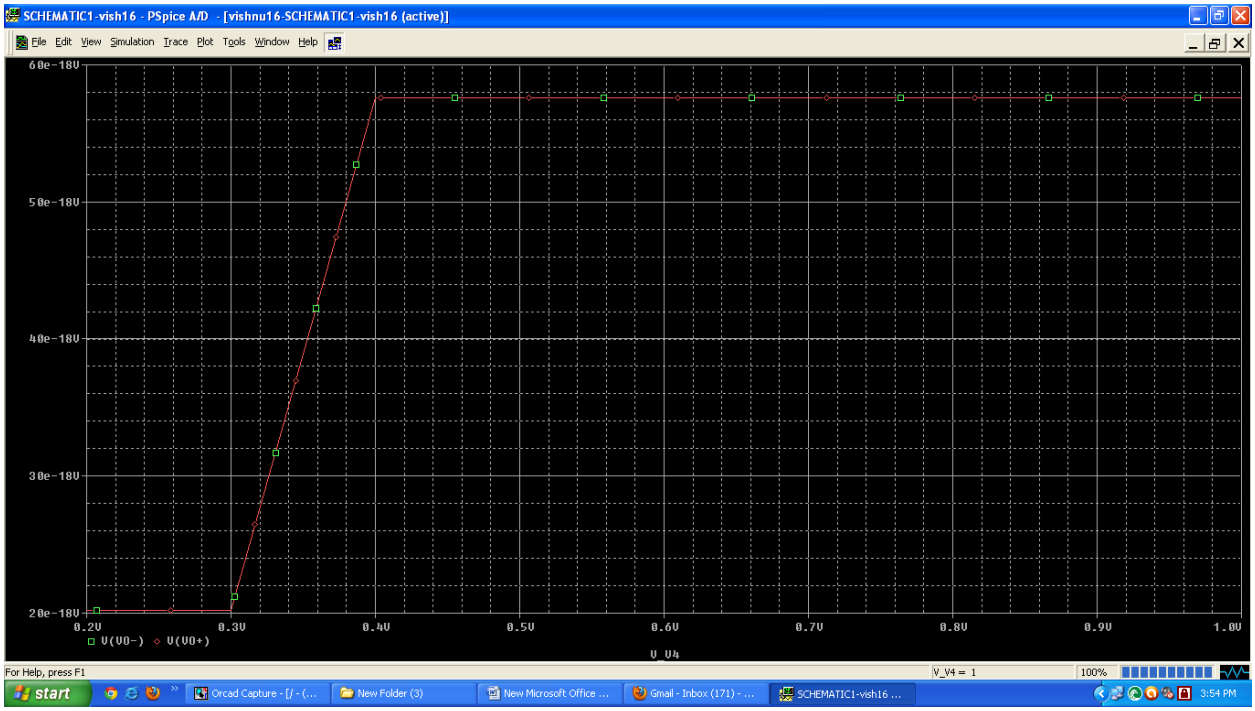

Fig. 3.offset voltage of conventional comparator vs. Vcm

PROPOSED COMPARATOR

The proposed comparator using a new dynamic offset cancellation technique is shown in fig-ure(4) and figure(5) shows its transient response obtained from simulation. It consists of double tail latched comparator, offset cancellation capacitors Cc+,Cc- and input switches Mb,MR1 and MR2.

In a reset phase, "sw" turns on, the common mode voltage Vcmi input to the gate of the transistor M1' and M2'. At the same time the bottom nodes of the capacitors Vcb connects the bias voltage Vb. The top node of the capacitors Vc+ and Vc- are charged up until when M1' and M2'are turns off therefore, voltages of the offset capacitors are given by

$$Vc+ - Vcb=Vcmi -Vth1-Vb$$
$$Vc- - Vcb=Vcmi -Vth2-Vb$$

Where Vth1= threshold voltage of the M1' and Vth2=threshold voltage of the M2'
When "sw" turns off, Cc+ and Cc- maintain these voltages. After the reset phase, "swt" turns on, the input nodes of the comparator connects to the input signal.

$$Vin+= Vcmi +dVin$$
$$Vin-=Vcmi –dVin$$

When VI turns on, comparator starts to compare the input voltage. After comparison Vr turns on to reset the offset canceling capacitor.

Input common mode voltage and the offset voltage of the comparator is shown in the figure (6). Same size transistors are used in both the comparators. Bias voltage (Vb) used in the proposed comparator is 100Mv.The offset voltage of the proposed comparator is lower than conventional comparator in all conditions. Voff in the proposed comparator equals 0.3µV while conventional one equal to 0.87µV in case of Vcmi=0.6V. When we changes Vcmi from 0.2V to 0.3V, it decreases by 0.57µV in proposed comparator. Other simulation conditions are same.

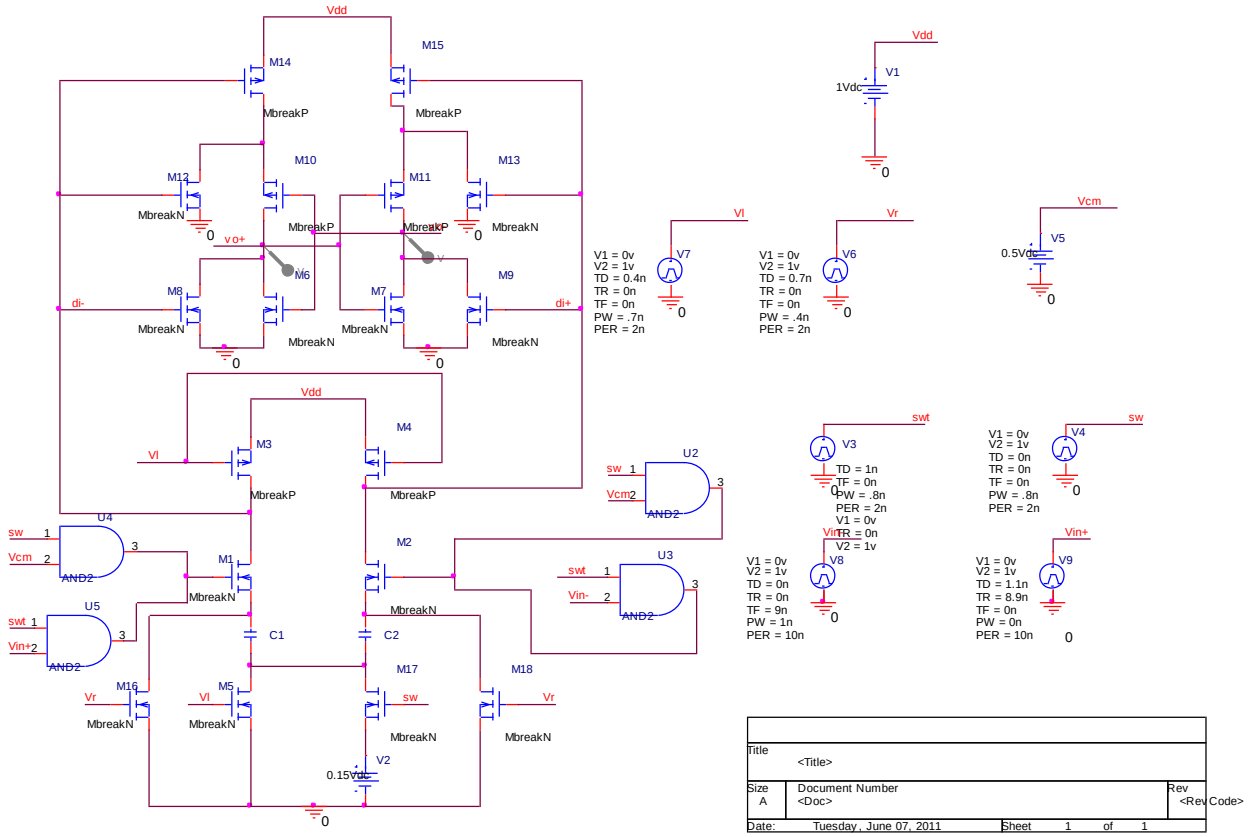

Fig. 4. The proposed comparator using dynamic offset cancellation technique.

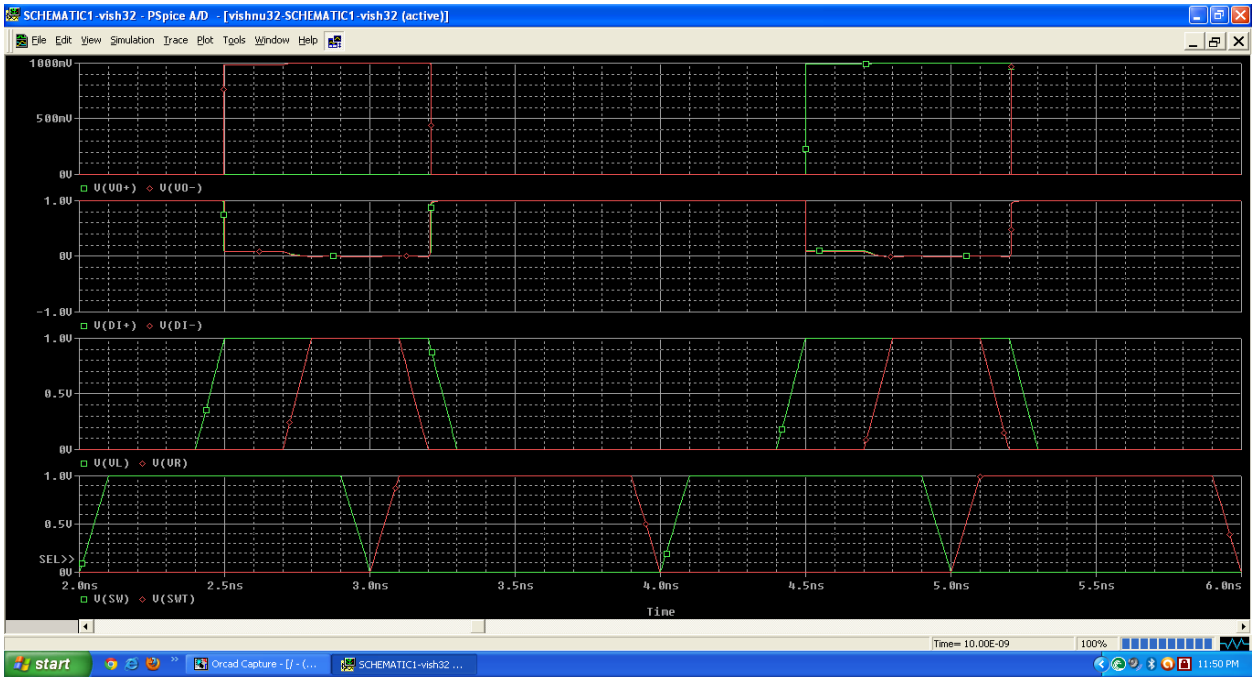

Fig.5. input and output waveforms of proposed comparator

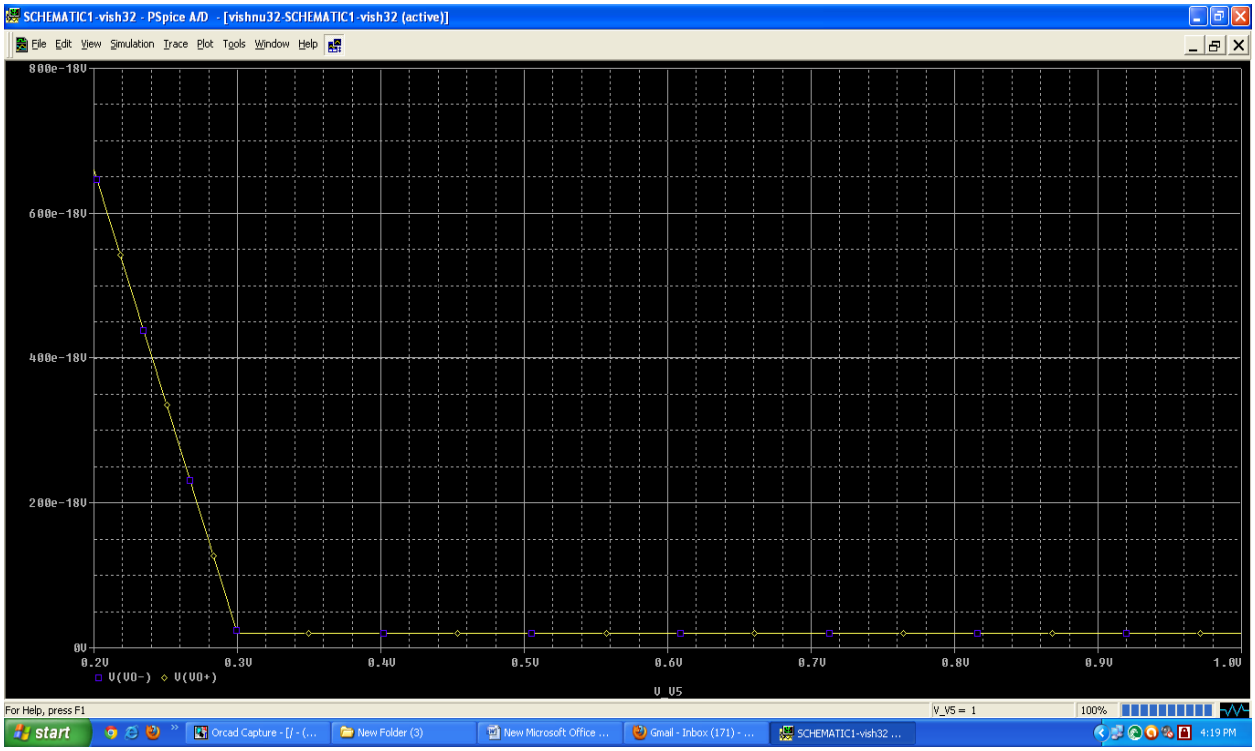

Fig.6.offset voltage of proposed comparator vs. Vcm

CONCLUSION-

A low offset, small area comparator using new offset dynamic offset cancellation technique is proposed. The proposed comparator consumes no static power. Measured results show the input offset voltage is improved from0.87µV to 0.3µV by using proposed technique at 500MHz conversion frequency.

Moreover the proposed comparator has an advantage that the offset voltage does not change by increasing the input common mode voltage compared with the conventional comparator. The offset voltage of the proposed comparator decreases by only 0.57µV when the input common mode voltage changes from 0.2V to 0.3V, in contrast to the 0.57µV increase for the conventional comparator.

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