A Review on Current-Mode CMOS Multiplier circuits with Improved Accuracy using Analog VLSI

Ansari Faheem Ahmed\(^1\), Shahezad Mobeen\(^2\), Siddiqui Mohsin\(^3\), Ashfaque Ahmed\(^4\), Rabiya Hamid\(^5\)

\(^{1,2,3,4,5}\) (E & TC Department, MMANTC, Mansoora, Malegaon/ SPPU, India)

Abstract: This paper is consisting on reviews of researches done on analog multipliers with better performances in many aspects. As there are two techniques exists in making analog circuits which are voltage mode approach and current mode approach, so taking the advantages of current mode techniques over voltage mode in mind in this paper we have reviewed only current mode analog multipliers. Analog multipliers since are useful in analog signal processing they have huge applications in our daily life devices and equipment, like watt meter, hour meter (power supply measurement), Densitometer, Acoustic Thermometer, oscillators and many more. These applications have their own interest as they are the part of the devices which Wegener all yuseinour daily life. The circuits made using current mode techniques are having better frequency response, low power consumption and also better temperature sustainability. We are also representing the working of two best current mode multipliers which we found, those are checked and implemented by 0.18um technology in Cadence Virtuoso and Hspice simulations of four waves.

Key words: Current mode, Rectifier, Cadence Virtuoso, Hspice

I. Introduction

A multiplier is a device that having three ports i.e. two is used for the as a input ports and one is used as a output port. The output of the multiplier is nothing but a multiplication of both inputs. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor, \( K \), which has the dimension of voltage. Multipliers have many applications in analog systems and circuits. Modulator and mixer in communication systems are early applications of this block. Newer applications of this block are usage in implementing neural network and fuzzy logic systems. In a general point of view, we can classify multipliers in two categories of voltage and current.

In MOS voltage mode multipliers are classified in eight categories according to transistor or region of operation, nonlinearity cancellation schemes, and signal injection method. But this classification does not include current mode multipliers. Current mode processing has more advantages than voltage mode. These advantages include wider bandwidth, more linearity, lower power dissipation, simple circuitry etc. Most of current mode multipliers which are implemented in transistor or level can be divided in two categories of strong inversion and weak inversion. Although there are multipliers which are proposed based on blocks like OTA, CCII and different types of CDTAs and its derivatives. But most of these use BJT transistors and are not optimized in the terms of power dissipation and area consumption.

Based on sub-threshold hold operated MOS transistors, the realization of multiplier/dividers requires simple architectures. So as to enhance the frequency response of the computational structures and to expand their 3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of MOS transistors biased in saturation. In multiplier structures, single-ended input voltages, the linearization of their characteristics being obtained by proper squaring relations between the input potentials. In order to implement the multiplication of two differential-input voltages, in multiplier circuits were described based on mathematical principles, similar to those used by the multipliers with single input voltages\(^{[1-5]}\).

II. Literature Survey

The first research is based on the multiplier with low power consumption and lower linearity errors by using current mode techniques in the CMOS multipliers. The result of this also shows the advantages of current mode over voltage mode. The researcher used the square law properties of the MOSFETs for designing the two new circuits which are able to multiply signals with better accuracy and low power consumption as well as simple architecture operates at low voltage input. There are two circuits presented and both perform well with current inputs. The circuits got improved in bandwidth due current mode where as it also get immune to temperature variations. The two circuits with the combinations of current mirrors and current sources are proposed.

Different W/L ratios and combinations of both nmos and pmos are used, circuitismadeon0.18umCMOSTechnology\(^{[1]}\)

I\(^{st}\) National Conference on Technology

Maulana Mukhtar Ahmed Nadvi Technical Campus (MMANTC), Mansoora, Malegaon Maharashtra, India
The research presents a low power CMOS analog multiplier with better performance and simple design considering ratios. This design has low power utilization and having good linearity due to this design is very effective to use in analog circuits. The experiment is done in the SPICE simulation. The proposed circuit is working on voltage mode with low linearity error of almost 0.71.09 percentage and with huge bandwidth performance of up to 1.98 1.02 Ghz. Circuit is also immune to noise effects, it is made on cadencetool.[2]

A CMOS analogue current-mode multiplier/divider circuit is presented, which is based on a dynamic biasing applied at the body terminal of MOS transistors operating in both saturation and triode. Multiplier creates a feedback loop due to which enhance the accuracy and also enhance current swing. The multiplier has been fabricated using a standard 0.18 um CMOS technology and it consumes almost 144 uW power. The next circuit is based on the re-using of the same functional core for two circuit functions i.e. signal gain with theoretical null distortions and signal squaring. The most important circuit complexity is implementing the core of the structure, which is made easy in the circuits, both circuit area and power consumption per each realized function is strongly reduced in this method. The overall error of the transconductance amplifier is 0.4 percent and the approximation error for the squaring circuit is 0.27 percent, in the condition of a low-voltage low-power operation (a supply voltage of 1.5V and a medium current consumption of 50uA for each implemented circuit function[3][4]

### III. Comparative Study of The Papers

From all the references which we had studied we found that on every parameters such as low power consumption, chip area, maximum bandwidth, linearity errors and technology used to make them, the multiplier which was designed by Cosmin Radu Popa in sixth reference is better of all. We have given all studied values of multipliers on every parameters in the tabular form given below with their authors. As we had found that among all ComminPopa’s multiplier was better we also had done the hand calculations and simulations of his proposed idea of making the multiplier, those simulations and hand calculations are also shown below, using which one can understand the working of the circuit.

#### TABLE: Comparative study of analog multipliers

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<td>4] C.A De La Cruz-Blas, G. Thomas-Erving, J.M. Algueta-Miguel, A. Lopez-Martin, “CMOS Analog current mode multiplier/divider operating in triode-saturation with bulk driven technique” ElseVier Integration the VLSI, 2017</td>
<td>0.18</td>
<td>1.8</td>
<td>1.5</td>
<td>144</td>
<td>4050</td>
<td>62</td>
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<td>5] Aram Bahramast, Syed JawadAzhari, SiavashMowlavi, “A NEW CURRENT MODE HIGH SPEED FOUR QUADRANT CMOS ANALOG MULTIPLIER” 24th Iranian Conference on Electrical Engineering (ICCEE), 2016</td>
<td>0.18</td>
<td>1.8</td>
<td></td>
<td>89.2</td>
<td>200</td>
<td>840</td>
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<td>6a) Cosminpopa, “Improved Accuracy Current-Mode Multiplier Circuits With Applications in Analog Signal Processing” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2014</td>
<td>0.18</td>
<td>1.2</td>
<td>0.75</td>
<td>79.6</td>
<td>600</td>
<td>60</td>
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<td>6b) Cosminpopa, “Improved Accuracy Current-Mode Multiplier Circuits With Applications in Analog Signal Processing” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2014</td>
<td>0.18</td>
<td>1.2</td>
<td>0.9</td>
<td>59.7</td>
<td>800</td>
<td>75</td>
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IV. Simulation result and Hand calculations

As in the reference number 6 by Cosmin Popa there are two design methodologies used, we are here presenting both of them with hand calculations and simulation results.

Design Methodology:

Expression of the output current in this design (in fig. 4.1) is \( I_{\text{out}} = ID_2 - ID_1 + 2I_0 \) (by circuit analysis). Which gives the result of multiplier/divider circuit equation: \( I_{\text{out}} = \frac{I_0}{I_1} \). For this circuit we first taken \( I_0 = 40 \, \mu \text{A} \) (fixed), \( I_1 = 0 \) to \( 10 \, \mu \text{A} \), \( I_2 = 10 \, \mu \text{A}, 20 \, \mu \text{A}, 30 \, \mu \text{A}, 40 \, \mu \text{A} \). And calculated the output current on simulation results as shown below in figure 4.2, as an example to understand for \( I_0 = 40 \), \( I_1 = 5 \), \( I_2 = 10 \) we got \( I_{\text{out}} = 20 \, \mu \text{A} \) which can be verified with results also from fig. 4.2 also.

![Fig. 4.1 First Design of multiplier](image)

**Fig. 4.1 First Design of multiplier**

For current \( I_2 \) we took \( I_0 = 40 \, \mu \text{A} \) (fixed), \( I_2 = 0 \) to \( 10 \, \mu \text{A} \), \( I_1 = 10 \, \mu \text{A}, 20 \, \mu \text{A}, 30 \, \mu \text{A}, 40 \, \mu \text{A} \) And found \( I_{\text{out}} \), for example For \( I_0 = 40 \), \( I_1 = 5 \), \( I_2 = 10 \) and got \( I_{\text{out}} = 20 \, \mu \text{A} \). This also can be verified by fig. 4.3

![Fig. 4.2 Iout vs I1 current simulation graph](image)

**Fig. 4.2 Iout vs I1 current simulation graph**

For current \( I_2 \) we took \( I_0 = 40 \, \mu \text{A} \) (fixed), \( I_2 = 0 \) to \( 10 \, \mu \text{A} \), \( I_1 = 10 \, \mu \text{A}, 20 \, \mu \text{A}, 30 \, \mu \text{A}, 40 \, \mu \text{A} \)

And found \( I_{\text{out}} \), for example For \( I_0 = 40 \), \( I_1 = 5 \), \( I_2 = 10 \) and got \( I_{\text{out}} = 20 \, \mu \text{A} \). This also can be verified by fig. 4.3

![Fig. 4.3 Iout vs I2 current simulation graph](image)

**Fig. 4.3 Iout vs I2 current simulation graph**

Author has also done transient analysis to get the frequency response of the circuit. In which he has taken \( I_0 = 200 \, \mu \text{A} / 1\text{MHz} \), and \( I_2 = 300 \, \mu \text{A} \), \( I_1 = 300 \, \mu \text{A} / 60\text{MHz} \) and output shown in below fig 4.4. Found linearity error less than \( 0.75\% \), can be observed in fig. 4.5
Design Methodology 2:

Expression of the output current in this design (in fig. 4.6) is \( I_{\text{out}} = I_{\text{out1}} - I_{\text{out2}} + 2I_0 \) (by circuit analysis). Which gives the result of multiplier/divider circuit equation: \( I_{\text{out}} = \frac{I_0}{I_1} - I_2 \). For this circuit, we first taken \( I_0 = 40 \mu A \) (fixed), \( I_1 = 0 \) to \( 10 \mu A \), \( I_2 = 10 \mu A, 20 \mu A, 30 \mu A, 40 \mu A \) and calculated the output current on simulation results as shown below in figure 4.7, as an example to understand for. For \( I_0=40, I_1=6, I_2=10 \), \( I_{\text{out}} = 24 \mu A \) which can be verified with results also from fig. 4.7 also.
For current I2 we took I0 = 40 µA (fixed), I2 = 0 to 10 µA, I1 = 10 µa, 20 µA, 30 µa, 40 µA and found Iout for example for I0=40, I2=6, I1=10. Iout = 24 µA. This also can be verified by fig. 4.8

![Fig. 4.8 Iout vs I2 current simulation graph](image)

Author has also done transient analysis to get the frequency response of the circuit. In which he has taken I0 = 200µA/1MHz, I2 = 300µA, I1 = 300µA/45MHz and output shown in below fig 4.9. Found linearity error less than 0.75%, can be observed in fig. 4.10

![Fig. 4.9 Transient analysis of multiplier](image)

![Fig. 4.10 Linearity error](image)

V. Conclusion

After learning about the analog multiplier circuits and comparing the work of different authors on this topic it shows that the work which has presented is containing the most improved multiplier and divider circuits in context to the low power consumption and low linearity errors but it lags in bandwidth and chip area is more.

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