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Design of Low Power 5T-Dual Vth SRAM-Cell

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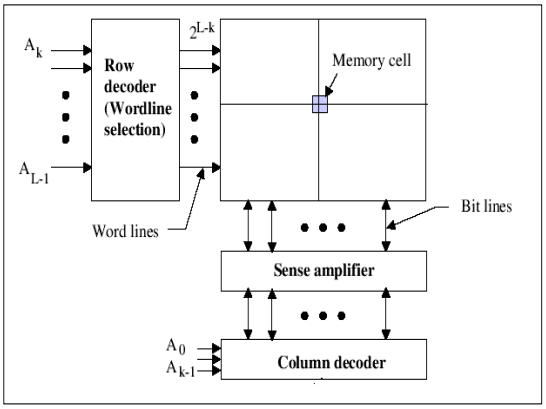
ABSTRACT
Semiconductor memories are most important subsystem of modern digital systems. In new era the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. But due to high density, power dissipiation gets increases and speed decreases. So there is need for the design of low power and high speed circuit in memory. This paper presents a 5-transistor dual voltage SRAM cell intended for the advanced microprocessor cache market using 1.8v/0.18um cmos technology. The goal is to reduce the power of the cache memory array while maintaining competitive performance. Various existing technologies are briefly discussed with their strengths and weaknesses. The design metrics for the 5-transistor cell are discussed in detail and performance and stability are evaluated. Finally a comparison is done between 6-transistor technology and the 5-transistor technology using dual Vth technique.

Keywords: **Semiconductor Memories, Dual-Vth, low power SRAM, cmos technology**.

1. INTRODUCTION
A memory in terms of computer hardware is a storage unit. There are many different types of hardware used for storage, such as magnetic hard drives and tapes, optical discs such as CDs and DVDs, and electronic memory in form of Integrated memory or stand-alone chips. The main focus of this Synopsis is the SRAM. There are four basic operations that have to be supported by a SRAM.

These are the writing and reading of '0' and '1' respectively. This is in contrast to read only memories (ROM) which only support the reading of '0' or '1'.



There are some very important requirements for a memory when it is to be embedded as on-chip cache. First and foremost it has to be reliable and stable. This is of course true for all memories, but is especially important for cache due to the more extreme performance requirements and area limitations. Secondly the memory has to have high performance. The sole purpose of cache is to speed up the operation of the CPU by bridging over the performance gap between main memory and the CPU. Another most important requirement is low power consumption. Today's advanced microprocessors use a lot of power and get very hot as a result. With increasing memory sizes these contribute with more and more power loss. This is especially important in mobile applications where prolonging battery life strongly depend on minimizing power loss.

Low power architectures are therefore chosen for cache memories and low leakage is taken into account when the sizing is done [2].

2. DUAL – Vth 6T-SRAM CELL – A typical dual Vth 6T-Cell is shown in fig-2. The access transistors M3 and M6 are controlled by the world line (WL).It threshold voltage of N3 and N4 is low , the switching time of N3 and N4 will be reduced, which will be reduced, which will in turns shorten the access time of the 6T- SRAM cell[4]

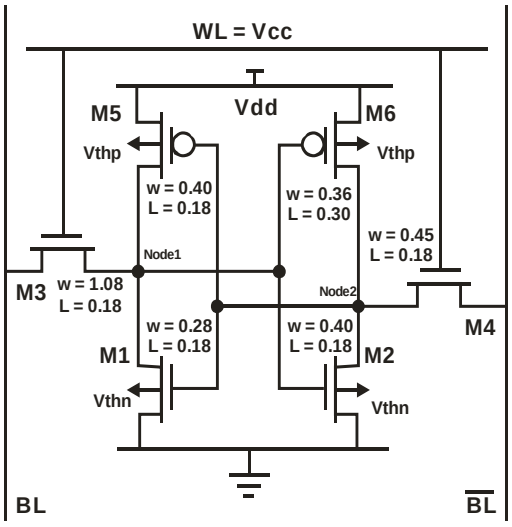


Fig-2 Schematic of Dual – Vth 6 -SRAM Cell with Final Sizes [1]

Hence we use the low-Vth transistors to implement the driving transistors. It will produce a large driving current than normal or high-vth transistors By contrast, transistors with high – Vth possess low leakage current and sub threshold current. Thus, they are very good to be cross coupled as a data latch. Thick channel transistors are showing high threshold voltage (high Vth), while thin channel transistors are showing low threshold voltage (low Vth) in fig shown below.
Design of 6T-SRAM Cell is started with making Schematic after that optimization of 6T-SRAM Cell is done is done in such a way that it meets the required objectives

3. DUAL – Vth 5T – SRAM CELL Fig-3 shows the dual Vth 6T-SRAM Cell with Final Sizes.

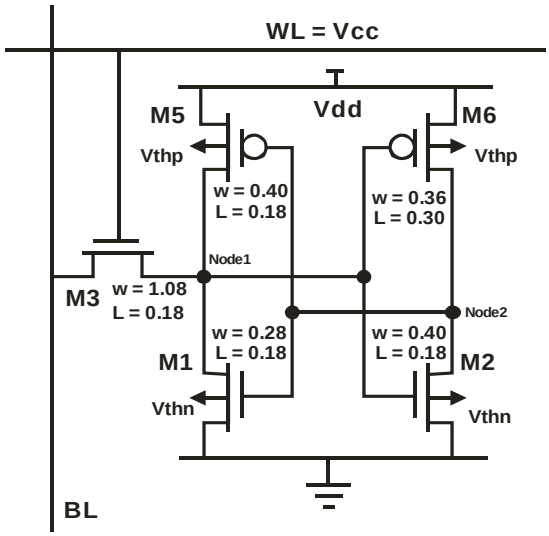


Fig-3 Schematic of Dual – Vth 5T-SRAM Cell with Final Sizes [1]

In this architecture Cross – Coupled transistors are high threshold voltage transistors.
To facilitate proper write operation, switching point of M2-M6 inverter should be lowered.

In conventional cells, this can be achieved by either making M2 stronger or M6 weaker. But in dual Vth SRAM cell we can use more facility by making P2, a high threshold voltage transistor in comparison to M2 transistors. [4]

Simulation results show a significant amount of power reduction by dual-Vth 5T-SRAM Cell in comparison to conventional 6T-SRAM Cell.
Design of 5T-SRAM Cell is started with making Schematic after that optimization of 5T-SRAM Cell is done is in such a way that it meets the required objectives

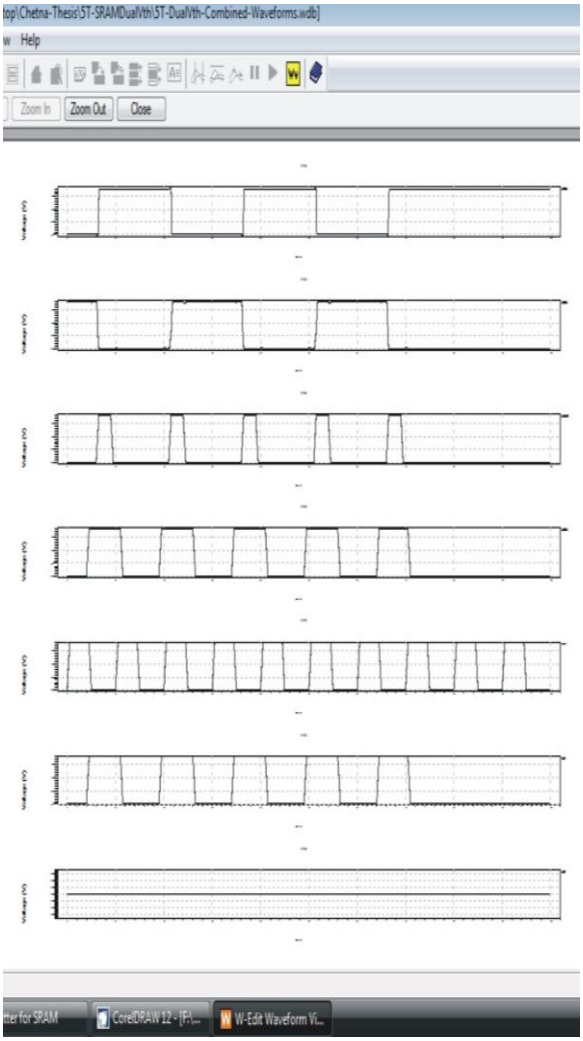


Fig- 4 Voltage Wave forms of Dual – Vth 5T-SRAM

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-2

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-1

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Word line

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Column

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Data

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Pre

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Vdd

Non-distractive write operation is possible for dual Vth 5T-SRAM cell with transistors sized for a 0.18um CMOS technology for proper write operation simulations are done for different width of transistor. The width is varied in steps of 0.04 um. The result of these simulations are shown in fig-5

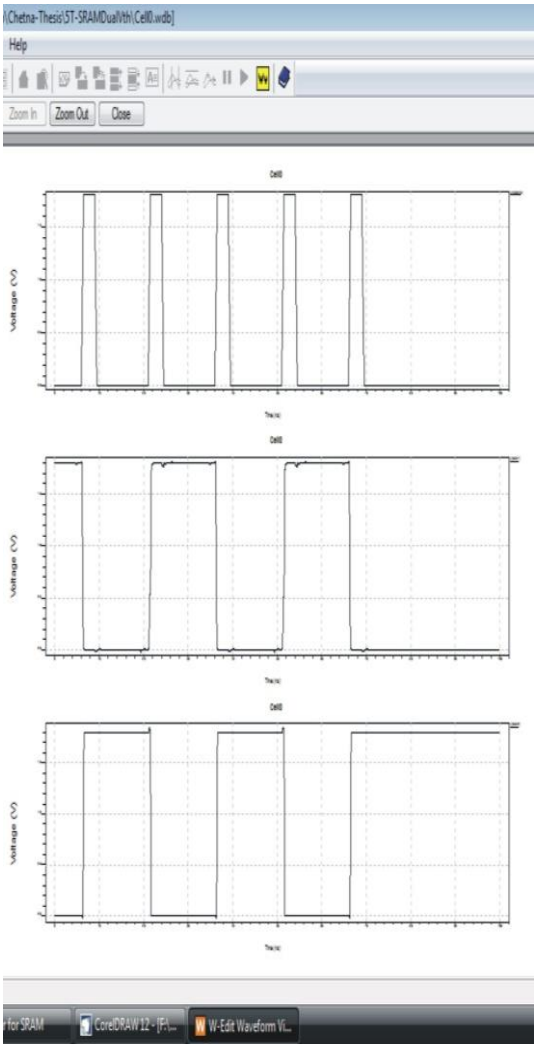


Fig-5 Simulation Wave forms of Dual – Vth 5T-SRAM

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-Word line

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-2

Voltage Signal of Dual – Vth 5T-SRAM Circuit at Node-1

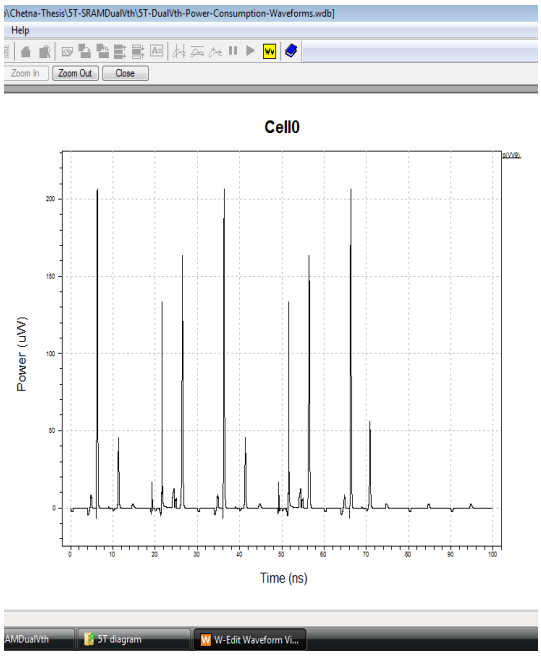


Fig-6 Write power consumption in dual Vth 5T-SRAM Cell

Table 1- Write delay in dual Vth 5T-SRAM

Operation	5T-SRAM Cell Write Delay(ns)
Write'0'	3.0038e-08
Write'1'	1.5351e-08

Table 2-Write power consumption in dual Vth 5T-SRAM

Operation Write Delay(ns)	5T-SRAM Cell Write Power Consumption (µw))
0	0
2.5	10
3.0	200

Average Power Consumption	**210(µw)**

Hence all of these parameters have adjusted together until a satisfactory result is achieved. For instance sizing of transistors have been done
In such a way that 5T- SRAM Cell can reduce power decapitations and delay shown in above tables.

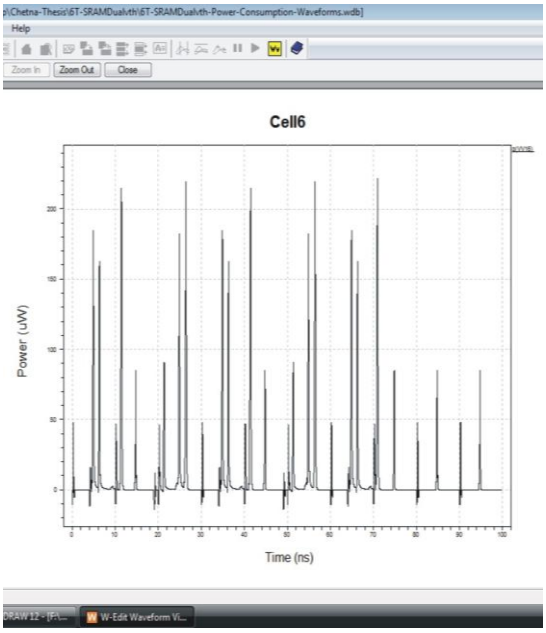


Fig-7 Write power consumption in dual Vth 6T-SRAM Cell

4. CONCLUSION

In this paper, the analysis and simulation is done for Dual - Vth 5T- SRAM Cell as compared with Dual - Vth 6T-SRAM Cell using 1.8v/0.18um cmos technology. The values of sensing delays and average power consumption are calculated for different sizes of CMOS-Transistors.

Table3- Comparison of Sensing Delay for Dual Vth 6T-SRAM Cell and Dual Vth 5T-SRAM

Operation	5T-SRAM Cell Write Delay(ns)	6T-SRAM Cell Writ Delay(ns)
Write'0'	3.0038e-08	3.0518e-08
Write'1'	1.5351e-08	1.5143e-08

Table4- Comparison of Average power consumption for Dual Vth 6T-SRAM Cell and Dual Vth 5T-SRAM Cell

Operation Write Delay(ns)	5T-SRAM Cell Write Power Consumption (µw))	6T-SRAM Cell Write Power Consumption (µw)
0	0	50
2.5	10	180
3.0	200	160
Average Power Consumption	210(µw)	390(µw)

The comparison table shows that the delays are marginally equal for Dual-Vth 5T-SRAM Cell and Dual - Vth 6T-SRAM Cell. But In case of Dual-Vth 5T-SRAM Cell bit line capacitance reduces due to single ended architecture and hence Average power consumption of Dual-Vth 5T-SRAM Cell is significantly less as compared to Dual - Vth 6T-SRAM Cell.

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