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Optimum Design of D-Latch for Low power Applications

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Abstract: Low-power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products. This research paper compares two designs of latches. Design comparisons are performed at 65nm and 45nm to show technology independence. Simulation results demonstrate the superiority of the 8T_1 latch design over 8T_2 latch in terms of power consumption at different temperatures, supply voltages and frequencies.

Keywords*— *Low power, Subthreshold region, portable applications, Level triggered flip-flop, latch.

I. INTRODUCTION

As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance is implemented in layout level, which develops the low power consumption chip, using recent CMOS, micron layout tools [1].

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for low power, high speed, small area, longer battery life and more reliable systems. This tremendous demand is due to demand and popularity of battery-operated portable equipments such as personal computing devices, wireless devices, medical applications and other portable devices. The continuous decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption [2] and [3].

VLSI Device design is being motivated by three basic goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed. Using less number of transistors is beneficial in reducing the number of components, interconnect parasitic capacitances, reducing chip area, lower propagation delay and potentially lower power consumption.

Latches and Flip-Flops are the most complex, power consuming and indispensible components among the various building blocks in digital designs. About 30%-70% of the total power in the system is dissipated due to clocking network, and the flip-flops [4]. The logic gate delays in a clock period is reducing by 25% per generation in high-performance microprocessors, and is approaching value of 10% or below beyond 0.13µm technology [5]. As a result, latency of the flip-flops or latches is becoming larger portion of the cycle time. Several FF designs have been proposed for power reduction. Although many of these methods have been shown to considerably reduce the power consumption, they are not necessarily suitable for operation in the sub-threshold region. In addition, some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of V_{TH}, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub-threshold operation.

Subthreshold current of an MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a subthreshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_{TH}, the circuit can be operated using the subthreshold current with ultra-low power consumption [6] and [7].

Subthreshold digital circuits will be suitable for the specific applications which need high performance as well as low power consumption. This type of application includes medical equipments such as hearing aids and pace maker, wearable wrist-watch computation, and self powered devices. It can also be applied to applications in which the circuit remains idle for an extended period or to portable applications which cannot carry heavy batteries. Minimizing power consumption is therefore important, both for increasing levels of integration and to improve reliability, feasibility and cost.

IC Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. Layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit [8]. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria. The layout step is the last major step in the design process before testing and fabrication.

This paper is organized as follows: Section II describes the 8T_1 latch reported in the literature. Section III describes the design and functionality of 8T_2. Simulation results, their comparisons and layout are presented in Section IV and finally Section V draws the conclusion.

II. LATCH DESIGN

A. 8T_1 latch design

The 8T_1 design implements pass transistor logic for the transmission of data through it [9]. The data input is connected to pMOS_1 and this data will be available at the output drain terminal only when the clock will be low. Thus this clocked latch acts as a negative level triggered flip flop.

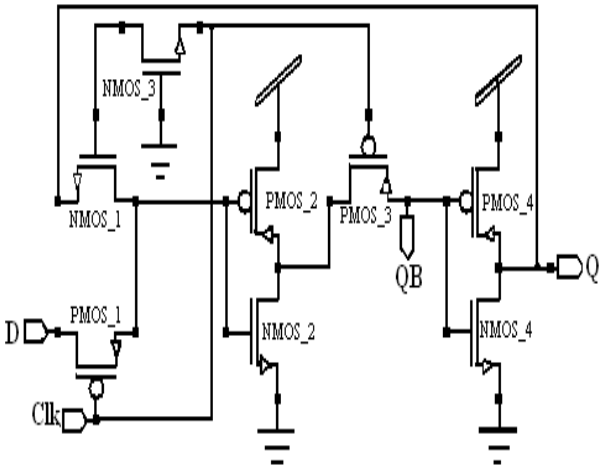

Figure 1. 8T_1 Latch Design

Since the PMOS transistors are weak zero transistor, so the small threshold loss is observed when data is zero. But overall performance of the device is almost unaffected because of the presence of the inverters.

The NMOS_3 transistor at the path works as a delay element on a charge sharing basis. For the purpose of delay element, nMOS is preferred over PMOS because NMOS has less resistance and hence shows less power consumption, and also NMOS is faster than PMOS. The transistor NMOS_1 acts as a feedback transistor whenever clock signal is high. This output is present at the input according to the delayed version of the clock. Thus whenever clock is high, data is not passing through the transistor PMOS_1 but output is again feedback through the circuit and output remains same. Whenever, clock is negative, the output changes with respect to data but remains constant as clock goes positive. The output remains unaffected even if clock is absent, thus the latch is static in nature.

B. 8T_2 design

The design of 8T_2 latch is also constructed by pass transistor gate logic [10].

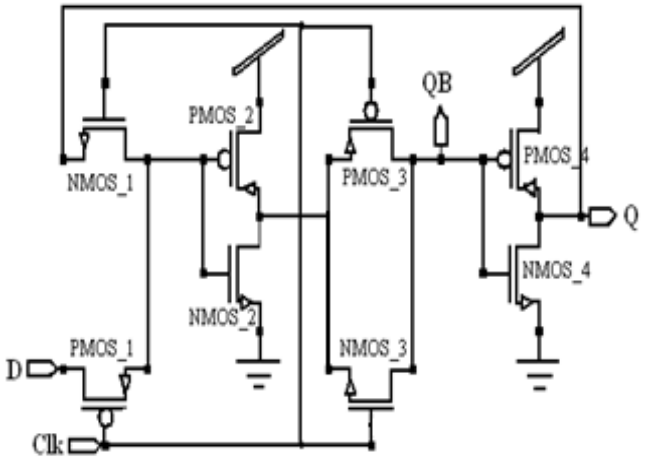

Figure 2. 8T_2 Latch Design

In this design, the transistor PMOS_1 at the input side takes the data and passes when the clock signal is low. The NMOS_1 is forming a feedback loop.

The transistor NMOS_3 is passing the output of the first inverter, when clock signal is high and transistor PMOS_3 is passing the signal, when clock signal is low. NMOS transistors are weak '1' and PMOS transistors are weak '0' transistors. Thus, pass transistor logic gives threshold loss problem. This problem is compensated by the two inverters in the circuit. Output 'QB' suffers with some threshold loss problem and that is verified during simulation, but output inverter compensates this problem and output waveform of 'Q' is not showing any threshold loss. The 8T latch is also negative level triggered.

III. SIMULATION AND COMPARISON

All schematic simulations are performed on Tanner EDA tool version 13.0 at 65nm and 45nm technology. The aspect ratio for all the transistors is taken unity for both designs.

The layout design for 8T_1 latch is shown in Figure 3 and the layout of the 8T_2 latch is shown in Figure. 4. The layouts have been designed for 65nm technology. The substrate terminals of all the circuits are connected to their respective source terminals in order to nullify the substrate-bias effect. The total number of parasitic capacitances is six in both the designs.

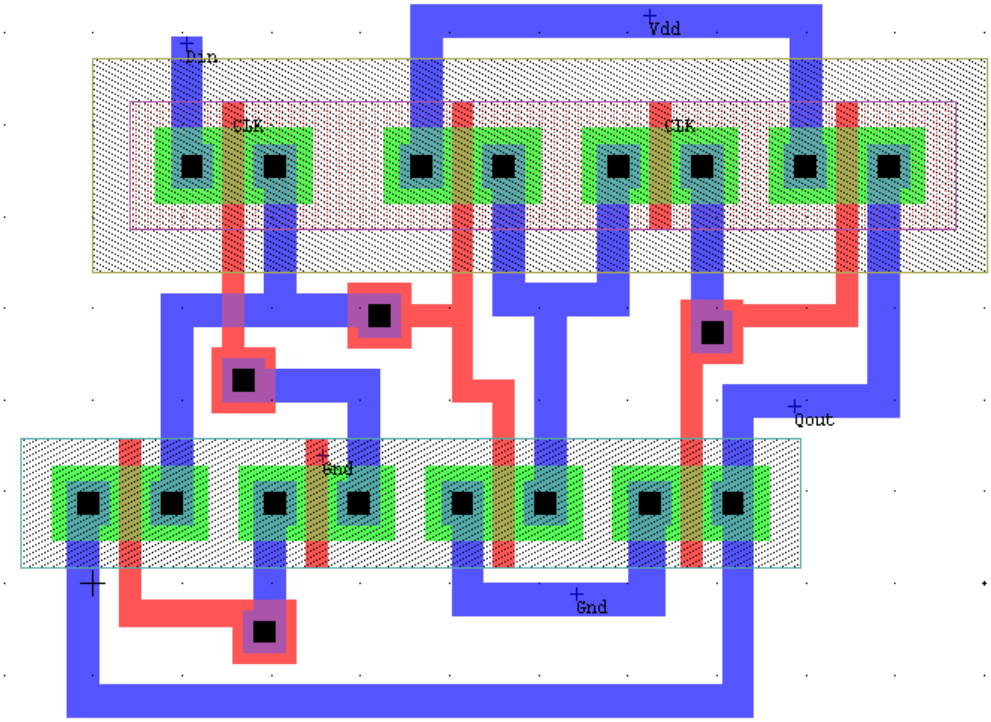

Figure 3. layout of 8T_1 latch

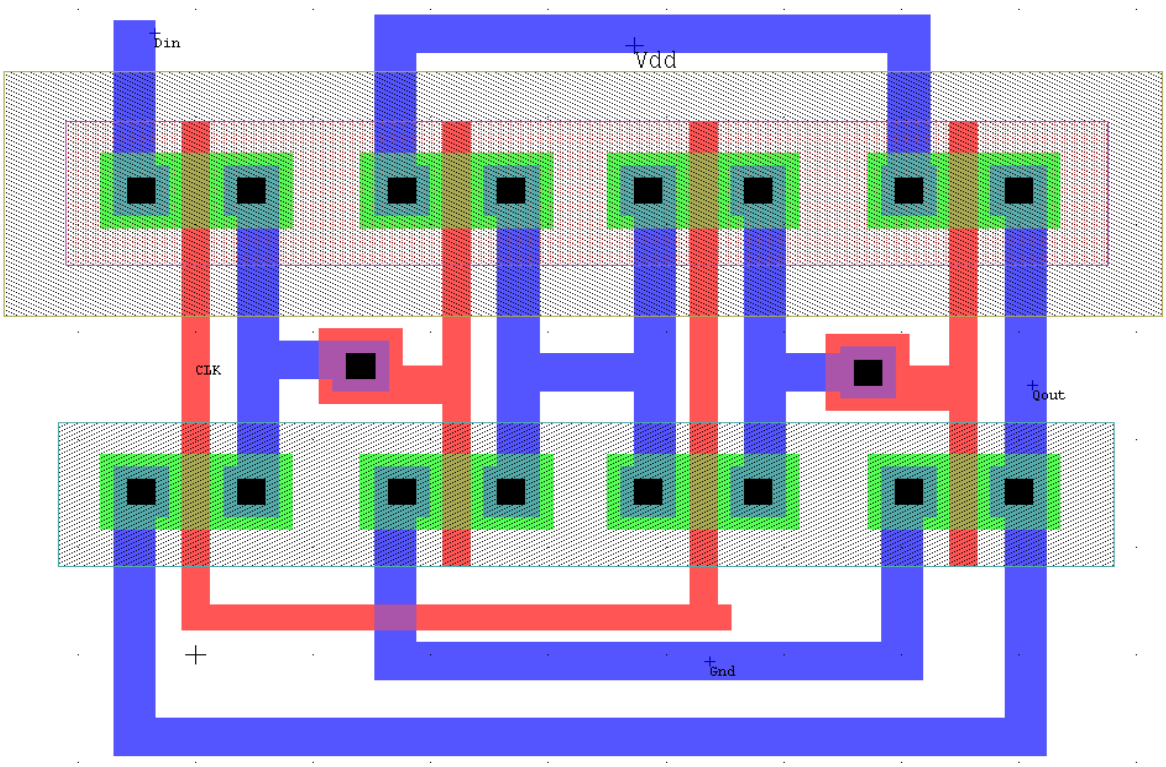

Figure 4. Layout of 8T_2 latch

Table I. Parasitic Capacitance of two latches

Parastic Capacitance	Parasitic Capacitance (F)	
	8T_1	8T_2
Total	7.150733E-16	5.744908E-16
Output	1.31783E-016	1.06193E-016

After the physical layout designing post-layout simulations are carried out with extraction of parasitic capacitances. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. So reduction in any one of these is beneficial. Table I shows significant reduction in total capacitance as well as output parasitic capacitances of 8T_2 latch.

The latch is analyzed in terms of power consumption at various supply voltages, frequencies and temperatures in subthreshold region. Power-Delay Product (PDP) is the function of power consumption as well as delay, so any reduction in average power consumption or delay will lead to overall reduction in PDP. To establish an impartial testing environment both circuits were simulated on same input patterns which covers each and every combination of the input stream. All simulation results are carried out by including 65nm and 45nm CMOS technology files in simulation environment.

A. Simulation results in 65nm technology

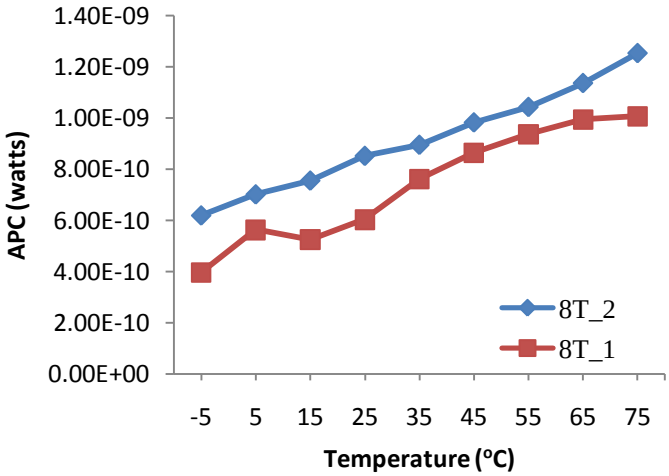

Figure 5. APC with increasing temperature

As temperature increases, than because of increase in thermal generation and recombination rate, the characteristics of the semiconductor device are affected. Thus, average power consumption of the device are affected with temperature as the collision rate of the carriers increases and some of the power is consumed in the form of thermal energy. From the above graph (Figure 5) it is clear that the power consumption of 8T_1 design is lower than 8T_2 design.

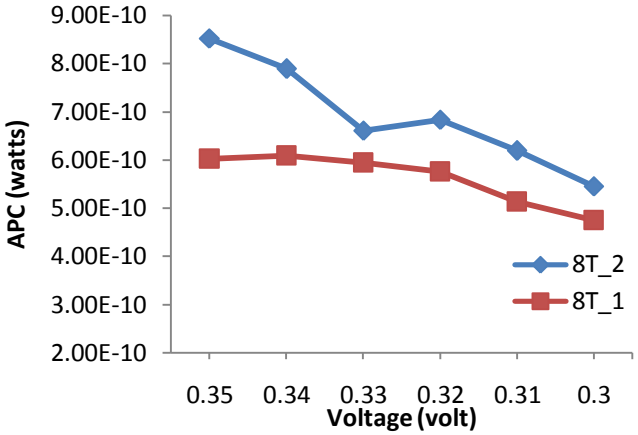

Figure 6. APC at different supply voltage

From Figure 6 it can be seen that power consumption of 8T_1 design is lower than 8T_2 design at different supply voltages. Simulations are performed in subthreshold region. Hence to ensure the working in subthreshold region, the input and supply voltages are kept the threshold voltage. Circuits operating in sub-threshold region are very sensitive to the supply voltage. Circuits operating in sub-threshold region are very sensitive to the supply voltage. The sensitivity to the average power consumption of the circuit increases with the decreasing power supply value.

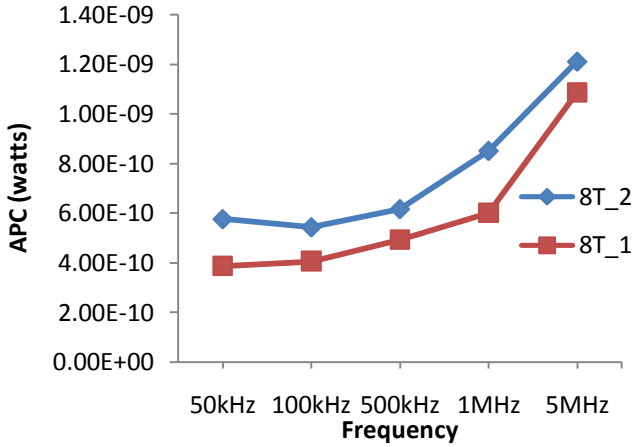

Figure 7. APC with increasing Frequency

As in sub-threshold region, circuits work better up to medium frequencies, hence range of frequencies are taken from 50 kHz to 5 MHz. Figure 7 shows the comparison of APC with increasing operating frequencies and it shows superiority of 8T_1 design over 8T_2 design in terms of average power consumption.

B. Simulation results in 45nm technology

Similar results are obtained when simulation is performed at 45nm CMOS technology.

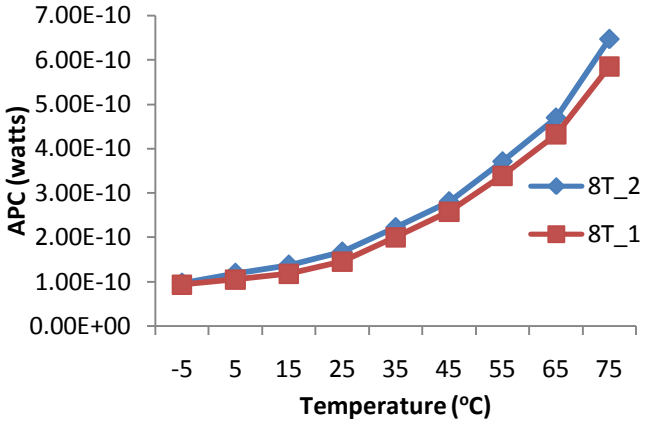

Figure 8. APC with increasing temperature

Comparison in terms of average power consumption with increasing temperature value is shown in Figure 8 and the result reveals that the 8T_1 latch has better temperature sustainability than 8T_2 latch.

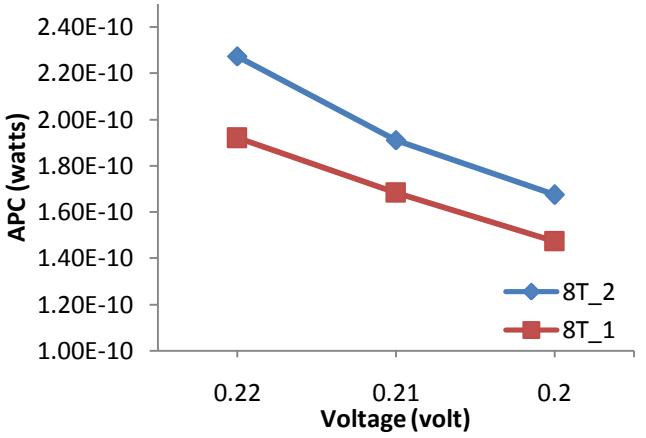

Figure 9. APC with varying input voltage and supply voltage

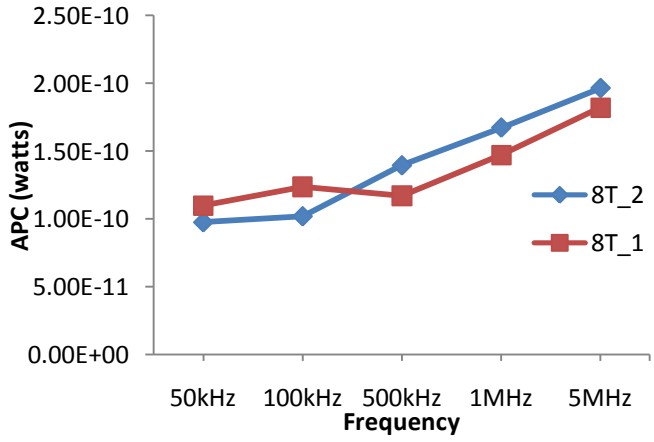

Figure 10. APC with increasing Frequency

Figure 9 depicts that the 8T_1 latch has reduced APC with increasing input and supply voltages when compared with 8T_2 latch.

Similarly Figure 10 shows the comparison of APC with increasing frequencies and it shows that for lower frequencies, APC of 8T_2 is lower but for higher frequencies, 8T_1 shows better results. The dynamic power component of the power consumption, i.e., $P = \alpha.C.V^2.f$, where α is the switching activity, is dominant at higher frequencies and becomes negligible at lower frequencies as the static power component takes over, i.e., $P = V_{DD} \times I_{Sub-threshold}$. Thus dynamic power component in 8T_1 and static power component in 8T_2 latch design is dominant in 45 nm technology.

IV. CONCLUSION

Low power consuming circuits are always first choice for any VLSI device construction. This paper compares the two earlier proposed designs of the two D latches. The simulation results shown in conjunction with design indicates that the 8T_1 design is power efficient than the 8T-2 latch design. Similarly the delay by the 8T_1 design is lower than the 8T_2 design resulting in the significant improvement in Power-delay product. Thus for systems where low power consumption and high performance is of primary interest within a certain power budget, 8T_1 latch design shows less power consumption and delay.

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