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2x2 Array Multiplier Based on DCVS Logic

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ABSTRACT

The Array architecture is a popular technique to implement the multipliers due to its compact structure. In this paper, 2x2 array multiplier circuits using existing full adder and DCVS logic full adder have been designed, simulated, analyzed and compared. An extensive analysis of multipliers has been done. According to our test results, an array multiplier designed by DCVS logic full adder is showing best result in terms of power consumption with varying supply voltage, temperature and operating frequency. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm technology.

Keywords: **Array multiplier, Full adder cell, High speed, 2:1 Multiplexer, VLSI**

I. INTRODUCTION

Multiplication is one of the basic arithmetic operations. In fact 8.72% of all instructions in a typical scientific program are multiplies. It is the most important operation in digital computer systems and digital signal processors. Digital multipliers are the most commonly used components in many digital circuit designs[1]. They are fast, reliable and efficient components that are utilized to implement any operation. The basic building block of the multiplier is the full adder cell, thus it has a significant effect on the overall performance and speed of the multiplier. Therefore, high speed full adders based on DCVS logic were presented .This one bit full adder is based on DCVSL 2:1 multiplexer.

II. DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC (DCVSL)

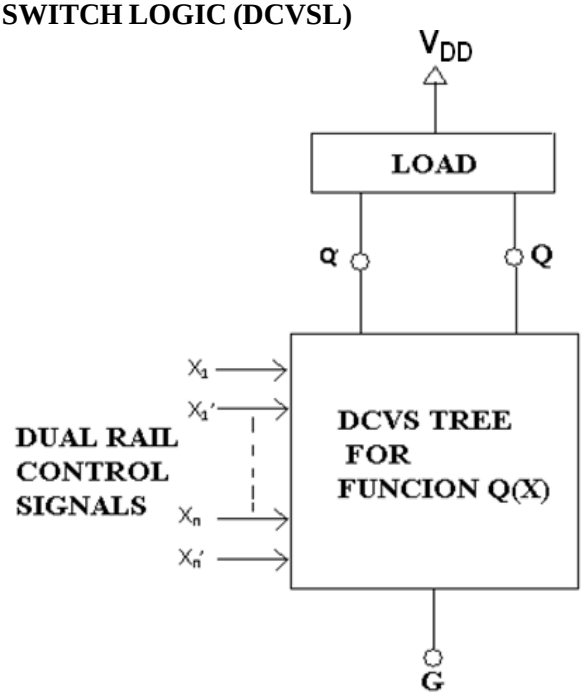

Fig.1 Basic DCVSL Circuit

One of the first realization of static differential CMOS logic known as the Differential Cascode Voltage Switch Logic (DCVSL) was introduced in 1984 [9]. Since then researchers have shown great interest in differential logic. This is due to its potential to efficiently realize complex logic functions. A logic function and its inverse are automatically implemented in this logic style. The pull-down networks implemented by the NMOS logic tree generated complementary output. The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. The basic DCVS circuit comprises two parts: a binary decision tree and a load. The tree is specified such that:

(1)When the input vector X = (Xl, . . . Xn) is the true vector of the switching function Q(x), then the output Q is disconnected from node G and the node Q' is connected to G; and

(2) When X =(X1... Xn) is the false vector of Q(x), and then the reverse holds. [2]- [4] Fig.1 shows the basic DCVSL Circuit.

The paper is organized as follows. First, Section II introduces the basics of Differential Cascode Voltage Switch Logic, Section III introduces the existing 2X2 array multiplier design then Section IV presents the designed 2x2 array multipliers, Section V shows simulations results and comparison and then finally conclusion is written in Section V.

III. EXISTING 2X2 ARRAY MULTIPLIER DESIGN

The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. A (A1, A0) and B (B1, B0) are 2-bit inputs given to multiplier giving output M (M3, M2, M1, M0). Fig.2 shows the basic architecture representing 2×2 array multiplier. It consists of four 2-input AND gates and

two 1-bit full adders. Multiplier design can be divided into two blocks, product generation and product addition. Product generation part built with the help of And Gate and product addition part built with the help of one bit full adder cell. Fig.3 shows the block diagram of existing 2x2 array multiplexer. This diagram contains 8 instances of CMOS inverter, 4 instances of NOR Gate and 2 instances of existing 1 bit full adder cell. The AND Gate formed with the help of CMOS. [5]

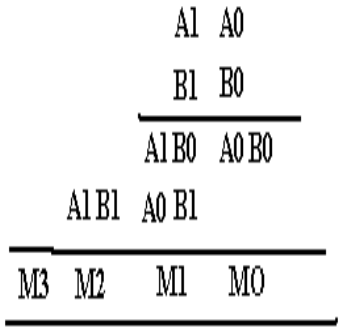

Fig.2 2X2 multiplication

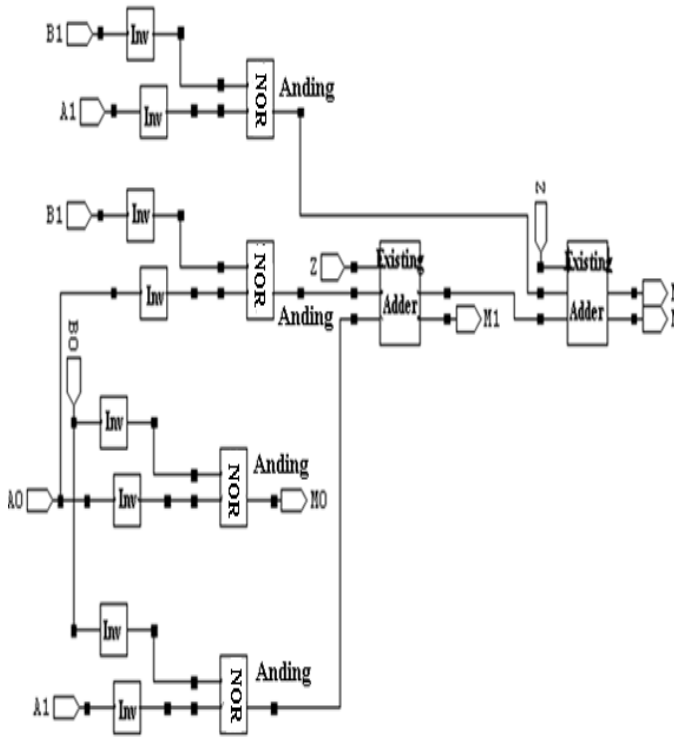

Fig.3 Schematic of existing adder circuit

inverter and NOR Gate. The schematic diagram and instances of inverter, NOR Gate and existing one bit full adder cell is shown in Fig.4, Fig.5, Fig.6, Fig7, Fig.8 and Fig.9 respectively.

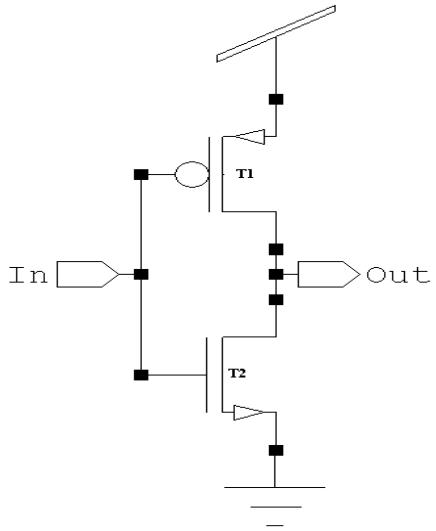

Fig.4 Schematic of CMOS inverter

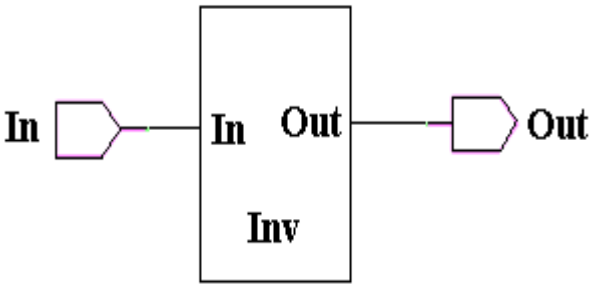

Fig.5 Instance of inverter

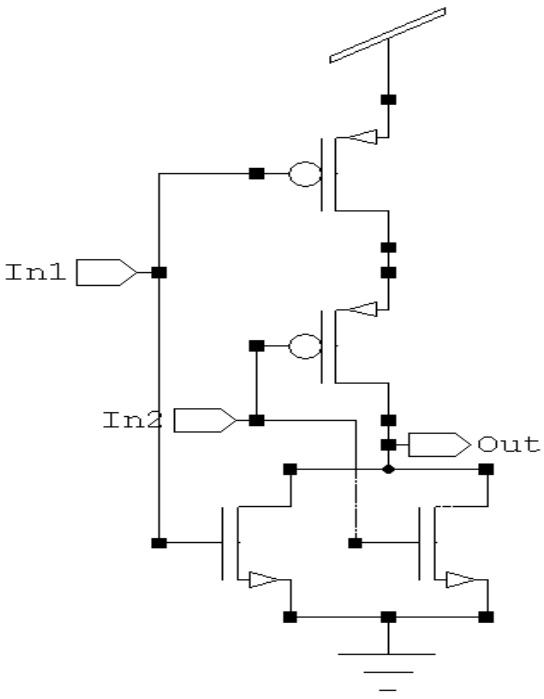

Fig.6 Schematic of NOR Gate

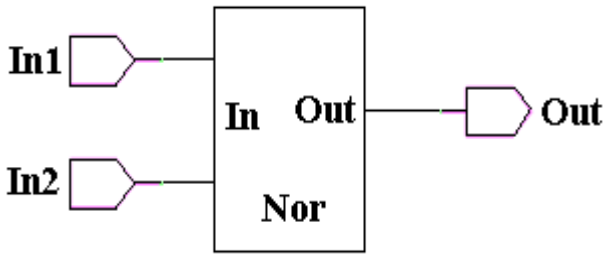

Fig.7 Instance of NOR Gate

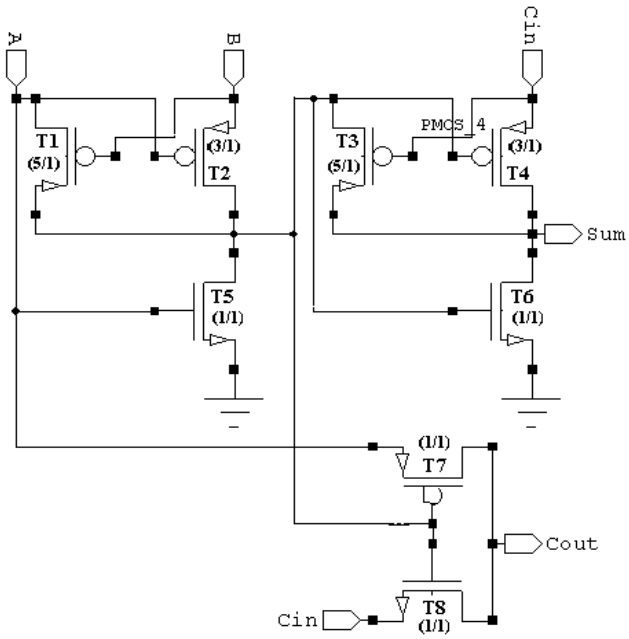

Fig.8 Schematic of existing adder circuit

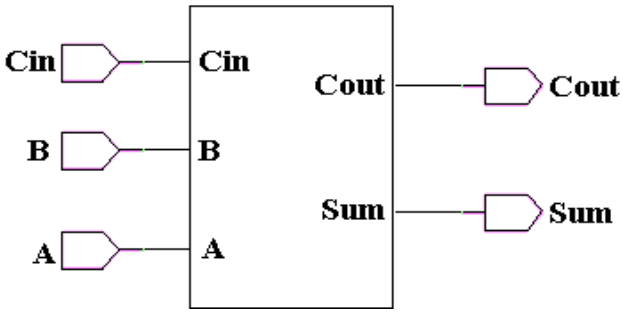

Fig.9 Instance of existing adder

IV. PROPOSED 2X2 ARRAY MULTIPLIER DESIGN

Fig.10 shows the block diagram of proposed 2x2 array multiplexer. This diagram contains 8 instances of CMOS inverter, 4 instances of NOR Gate and 2 instances of DCVSL based one bit full adder cell. The instance and schematic of DCVSL based one bit full adder cell is shown in Fig.11 and Fig.12 respectively.[6]-[10]

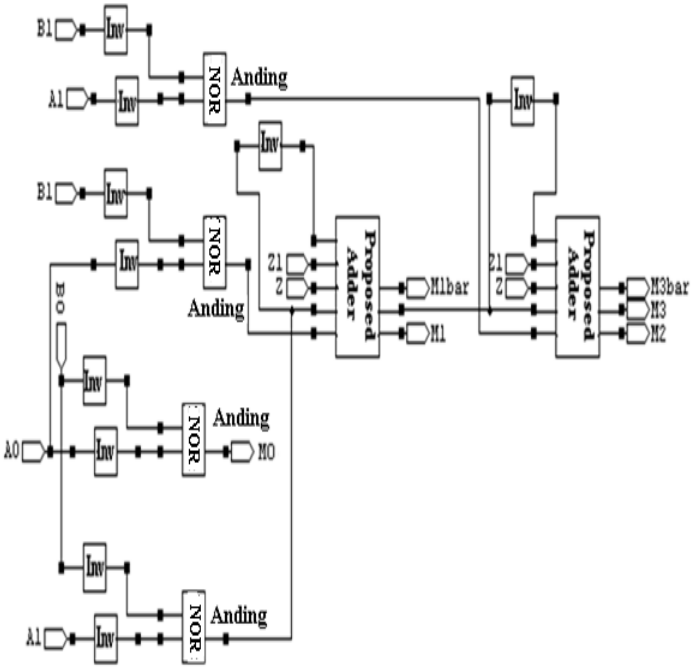

Fig.10 Block diagram of proposed 2x2 multiplier

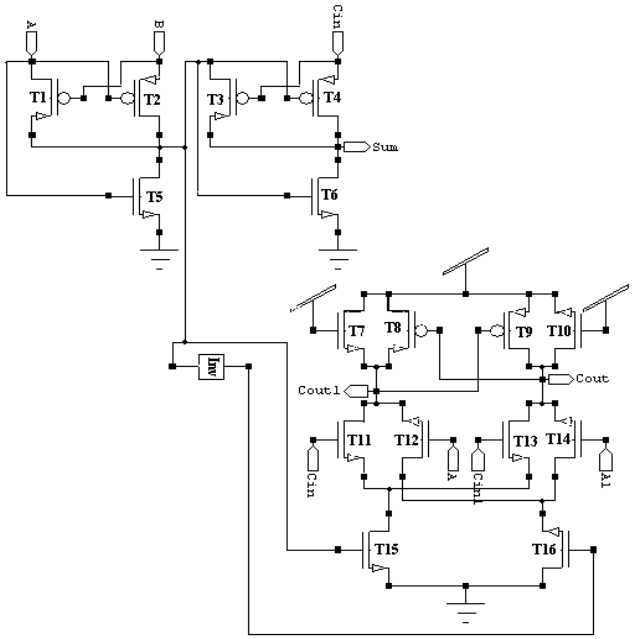

Fig.11 Schematic of adder circuit using DCVSL based 2:1 multiplexer

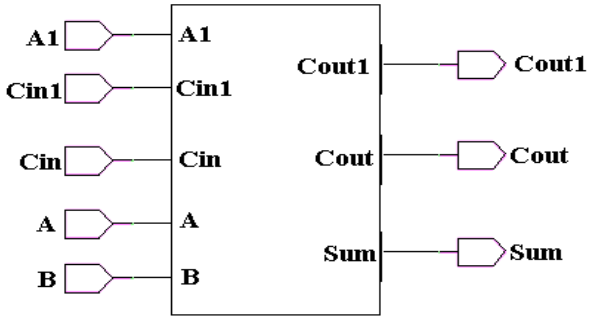

Fig. 12 Instance of DCVSL based adder

V. SIMULATIONS AND COMPARISON

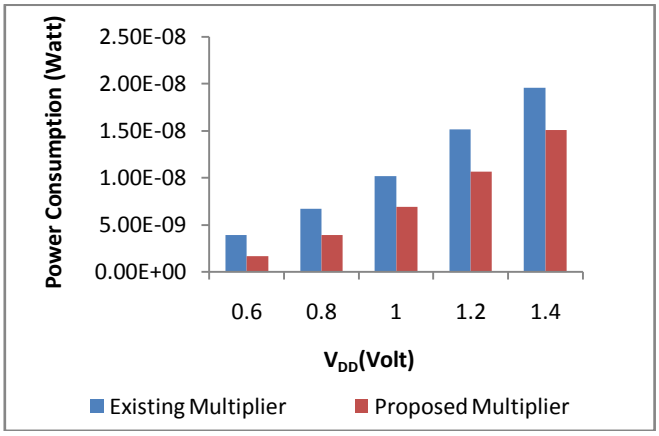

Fig.13 Power consumption comparison of existing and proposed multiplier at different supply voltages

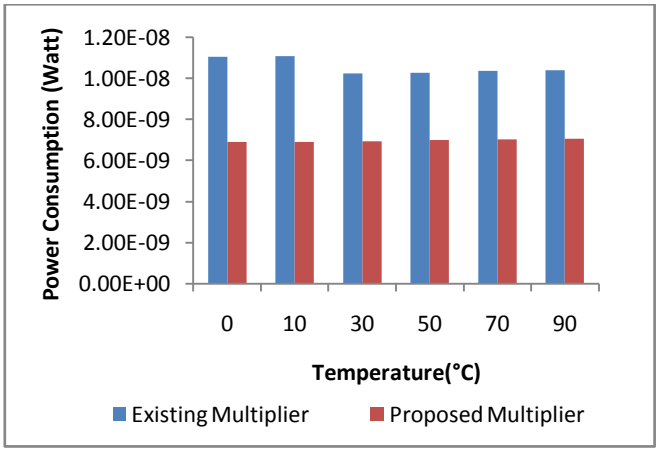

Fig.14 Power consumption comparison of existing and proposed multiplier at different Temperatures

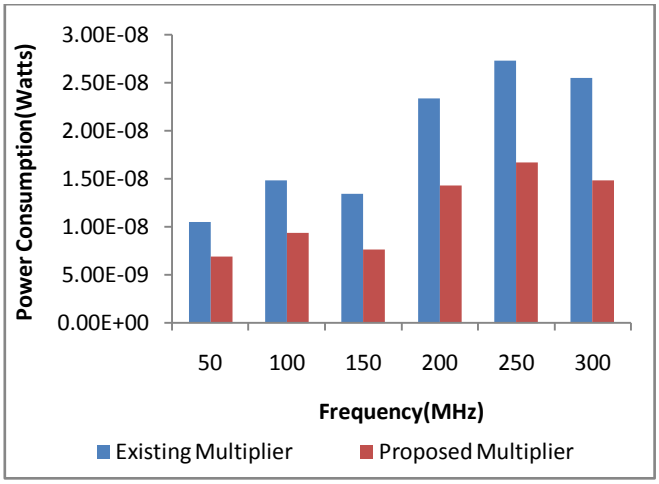

Fig.15 Power consumption comparison of existing and proposed multiplier at different frequencies

The pre-layout simulations are done at 90 nm technology. Graphs shown in Fig.13–Fig.15 depicts that the proposed 2x2 array multiplier is the viable option for efficient design. The graph shown in Fig.13 reveals that the power consumption of proposed 2x2 array multiplier is remarkably less than the existing 2x2 array multiplier for the input voltage ranging from 0.6V to 1.4V. Fig.14 and Fig.15 show graph between power consumption vs. temperature and power consumption vs. frequency, which shows proposed 2x2 array multiplier based on proposed 2:1 multiplexer has better performance.

VI. CONCLUSION

The 2X2 array multiplier based on DCVSL one bit full adder cell gives better performance than the existing 2X2 array multiplier. The 2X2 array multiplier based on DCVSL one bit full adder cell has been tested and it shows better performance at different temperature and frequency. It shows less power consumption to achieve high performance. It has been designed using 90nm technology and proved it to be a better option for low power complex system design. The net effect is that 2X2 array multiplier based on DCVSL one bit full adder cell shows a much better performance compared to 2X2 array multiplier.

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