IOSR Journal of Engineering (IOSRJEN) **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
Vol. 13, Issue 11, November 2023, ||Series -I|| PP 01-04

Threaded Summary Of Research On MOS Devices

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Abstract:*This article strings together all the research studies performed by the author in the period of 1996 to 2023 mainly in the area of Metal-Insulator-Semiconductor (MIS) characterization of the Metal-Oxide-Semiconductor (MOS) devices on 4H-SiC semiconductor except the formulated generalized MIS characterization technique called BOEMDET that is published elsewhere. The author was engaged in two Research Associate positions in USA as the starting point of the above research studies which continued to the present after returning to India in November, 2001.*
Keywords: *MOS Device, Silicon Carbide Semiconductor, Capacitance and Current-Voltage Characterization.*

I. Summary of Research

The current-voltage (I-V) characteristic through a metal-oxide-semiconductor (MOS) device has two regions of current that can be studied to provide an understanding of science of the MOS device. There is a high field region that occurs after the onset of the Fowler-Nordheim (FN) carrier tunneling and there is the low field region before the FN onset of carrier tunneling with the FN onset field being the field at which the ionization of the thermal SiO_2 begins.

FN hole tunneling current was first observed by the author in the year 2000 while studying the I-V characteristics of the MOS device fabricated on the (0001) oriented 4H-SiC semiconductor terminated with Si [1]. The hole barrier at the anode of the p-MOS device in accumulation was 2.915 eV and the electron barrier at the Au cathode with the SiO_2 conduction band (CB) was 4.2 to 4.4 eV. These barriers resulted in the dominant hole tunneling current from the anode into the oxide valence band (VB) in the two-terminal device [1]. The hole effective mass in the oxide was first found to be 0.35m in the year 2000 which was less than the established electron effective mass in the oxide of 0.42m. The value was later corrected to be 0.58m in the year 2011 when it was correctly imagined that the magnitude of the negative flatband voltage across the oxide that represents positive charges has to be added to the positive applied voltage at the anode to find the correct oxide voltage for the case of hole tunneling from the anode [2]. Four equations for the oxide voltage were formulated , two for the electron tunneling from the cathode of the MOS device having positive or negative charges in the oxide, and two for the hole tunneling from the anode of the MOS device having positive or negative charges in the oxide [2]. The average oxide fields for a charged MOS device was later on derived giving four equations that could be written as a single equation:

$$V_{ox} = V_{app} - V_{fb} \qquad (1).$$

Here, V_{ox} is the corrected oxide voltage, V_{app} is the applied voltage and $V_{fb}$is the flatband voltage obtained from the capacitance-voltage (C-V) characteristics across the MOS device. V_{app} is negative for electron tunneling from the cathode, and is positive for hole tunneling from the anode. The flatband voltage is negative for positive charges in the oxide and positive for negative charges in the oxide. Thus, four equations of corrected oxide voltages are possible that can be written as one equation presented above [3]. The CB offset was determined to be 2.7867 eV with the electron effective mass in the SiO_2 as 0.42m. The 2.7867 eV CB offset added to the 4H-SiC experimental bandgap of 3.234 eV gave the VB offset from the 4H-SiC VB to the oxide bandgap equal to 6.02 eV. This was very close to the VB offset determination by Afanasev et al. in 1996 of 6.0 ± 0.1 eV [4]. They used a transparent Au anode known not to oxidize in air. The oxide voltages at the cathode were found to be negative of the oxide voltages at the anode showing charge symmetry where Noether's theorem was applicable with the translation and rotation symmetries already being present in the Gauss's law used for finding the oxide voltages [5]. The MOS device on the C-face of 4H-SiC was also characterized for the CB offset. It was found to be 2.915 eV. CB offset on the C-face was the VB offset on the Si-faced MOS device. The difference in energy between the CB and VB offsets in Si-faced MOS device is thus 0.1283 eV that can be rounded to 0.13 eV [6]. The difference in the ground state energies of the electrons in the Si and C atoms of a tetrahedral bonded 4H-SiC as bilayers of Si and C is also found to be 0.13 eV [7]. Thus, the minimum number of bilayers of Si-C that exhibit the bulk bandgap of 4H-SiC becomes 25 starting with a Si layer and ending in a C layer, and 25 x 0.13 eV = 3.25 eV is the bandgap of 4H-SiC. The density functional theory gives the bandgap of 3.26 eV for the 4H-SiC [8-9]. The low field I-V characterization of the 4H-SiC MOS device also led to the determination of a new method of finding the near-interface trap density in the oxide or border trap density in the oxide near the CB utilizing an n-type MOS device and the formula for the density was

derived. Border traps in the oxide near the oxide/semiconductor interface were found in the 4H-SiC and Si MOS devices [10-12]. The charge density in the SiC MOS devices were found to be three times more than in the Si (111) MOS device because of the C present at the interface in the SiC MOS device. The C at the interface of SiC/oxide has two less electrons than O atom at the interface of Si/SiO_2 giving three times more positive charges [13]. Furthermore, after NO annealing and N incorporation the charges double because N replaces one O which has one less electron. Thus, the total interface trap charge density at or near the oxide/semiconductor interface (within 3 nm mean free path for electrons in the silicon dioxide) that communicates with the semiconductor increases six times from 4 x 10^{11}/cm^{2}eV at the Si (111)/SiO_2 interface to 24 x 10^{11}/cm^{2}eV at the 4H-SiC/SiO_2 interface for the p-type 4H-SiC MOS device. Nothing much can be done about this low 10^{12}/cm^{2}eV trap charge density which limits the n-channel mobility in the lateral MOSFET on (0001) oriented 4H-SiC to about 45-50 cm^2/V-s. Some bulk defects such as $Z_{1/2}$ and EH_5 in the 4H-SiC also show up as interface states in the MOS devices due to their high volume density [14]. Another research study showed that the conduction band offset (CBO) at the Si/SiO_2 interface of a Si MOS device remains the same as in the MOSFET device in inversion where due to quantization of the energy levels, the ground state energy level is at 0.2 eV at the surface where most of the electrons reside. The experimental threshold voltage for inversion in the MOSFET device is 0.4 V more than the theoretical threshold voltage. This translates to extra conduction band-bending at the surface of 0.2 eV. This extra band-bending nullifies the ground state energy position of 0.2 eV keeping the CBO same as in the MOS device at 3.2 eV at the semiconductor surface [15].

The high-field I-V helped in determining the effective mass of holes in the oxide from the slope constant of the current voltage characteristics through the MOS device at high fields and the CB offset of the oxide/Si interface and the low field I-V helped in determining the border trap density in the oxide near the interface. The FN onset field separating the low and high field currents is the onset of ionization in the SiO_2. The ionization characterization also gave the mean free path in thermal SiO_2 as 3.2 to 3.4 nm. The FN onset field is twice the CB offset in magnitude [16]. The ionization of SiO_2 produces electrons exponentially in the oxide that results in a diffusion current of electrons towards the anode. This diffusion current is the FN tunneling current at high electric fields showing wave-particle duality as the tunneling current is a wave behavior and the diffusion current of electrons is a particle behavior [17-18]. A simple model for the temperature dependence of the FN tunneling current was also derived with experimental corroboration. It gave a barrier height variation in 4H-SiC with temperature of -2.9 x 10^{-4} eV/K which is a very small variation and does not affect the oxide reliability significantly up to about 450 K temperature [19-20]. Further research showed that a MOS device alone can give a good estimate of Coulomb scattering limited channel mobility in a MOSFET device because the total interface states in a MOS device are inversely proportional to the mobility. So, if the total interface state density of one device, say a Si MOSFET is known for a known determined mobility, then with the inverse relation, the mobility of a device having a certain total interface states density can be found out using the formula:

$$\frac{\mu_1}{\mu_2} = \frac{D_{it2}+D_{NIT2}}{D_{it1}+D_{NIT1}} \qquad (2).$$

Here, D_{it} is the interface trap density and D_{NIT} is the near-interface trap density in the oxide near the semiconductor conduction band also known as the border trap density. The sum of the D_{it} and D_{NIT} forms the total interface trap density [21]. The above research led to a prediction of a viable low voltage power MOSFET on 2H-GeC having a plasma-enhanced chemical vapor deposited (PECVD) oxide. The 2H-GeC semiconductor is not available yet in a wafer form and it has an adversity of being expensive because of the involved rarer element Germanium [22]. Two more topics were researched namely, the ultra-thin oxide thickness determination and the photoluminescence based sensor device utilizing SiO_2 or high-K oxides modeled as direct wide bandgap semiconductors [23-24]. A review of the oxidation and annealing conditions on SiC is conducted, and it is proposed that an ultra-dry oxidation with less than 1 ppm water in the oxidation ambient can reduce the near-interface trap density by about 6 times to 4 x 10^{11}/cm^2-eV [25-26].

Pioneering work on 4H-SiC n-channel power MOSFET was done in a collaborative effort in the years 2000-2001 in USA as a Research Associate at the Vanderbilt University for one year. Lateral MOSFET was fabricated on (0001) oriented and Si-terminated 4H-SiC semiconductor having both dry and wet oxide by the Auburn-Vanderbilt Universities research group members in USA. The oxide/semiconductor interface was annealed in nitric oxide to incorporate N at the interface that reduced interface trap density at 0.1 eV below CB to 2 x 10^{12}/cm^{2}eV from 2 x 10^{13}/cm^{2}eV. The field-effect channel mobility obtained was 30-35 cm^2/V-s [27-28]. Ammonia was also tried as a gas to passivize the interface with N but was found to incorporate more N [29]. Later it has been found that N is incorporated in the bulk oxide as well when using NH_3 gas for passivation of the oxide/semiconductor interface. This lowers the oxide bandgap due to SiON formation and increases the leakage current in the oxide.

Another collaborative study at a GaAs MMIC company in Massachusetts, USA was performed on GaAs MESFET where it was determined that the MESFET with a thicker buffer layer of 0.5 micron was more

reliable in terms of breakdown strength as compared to the MESFET with thinner buffer layer of 0.3 micron [30].

In 2023, two research studies were done. In one, the bending of starlight by the sun's gravity was formulated which proved the equation of General Theory of Relativity of Einstein to be correct [31]. In the second study it was shown that 10^{28} eV particle energy is needed to unify the force of gravity with that of electromagnetism [32]. This would further the unifying of all the four forces of nature. The four forces of nature are: the force of gravity, electromagnetism, weak and strong nuclear forces. Another research study of 2013 is included in this threaded summary of research where a Hall-effect sensor is shown to be used to trip a relay [33]. Lastly, a research study of 2023 presents the philosophy of truth-seeking as part of human consciousness [34].

II. Conclusions

The above threaded research summary binds the studies by the author in one paper providing accumulated knowledge in one place to ease referencing about the author's studies and also highlight them.

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